

# Compal Confidential

Intel Haswell rPGA Processor with Lynx Point-H

www.aitech1.ru

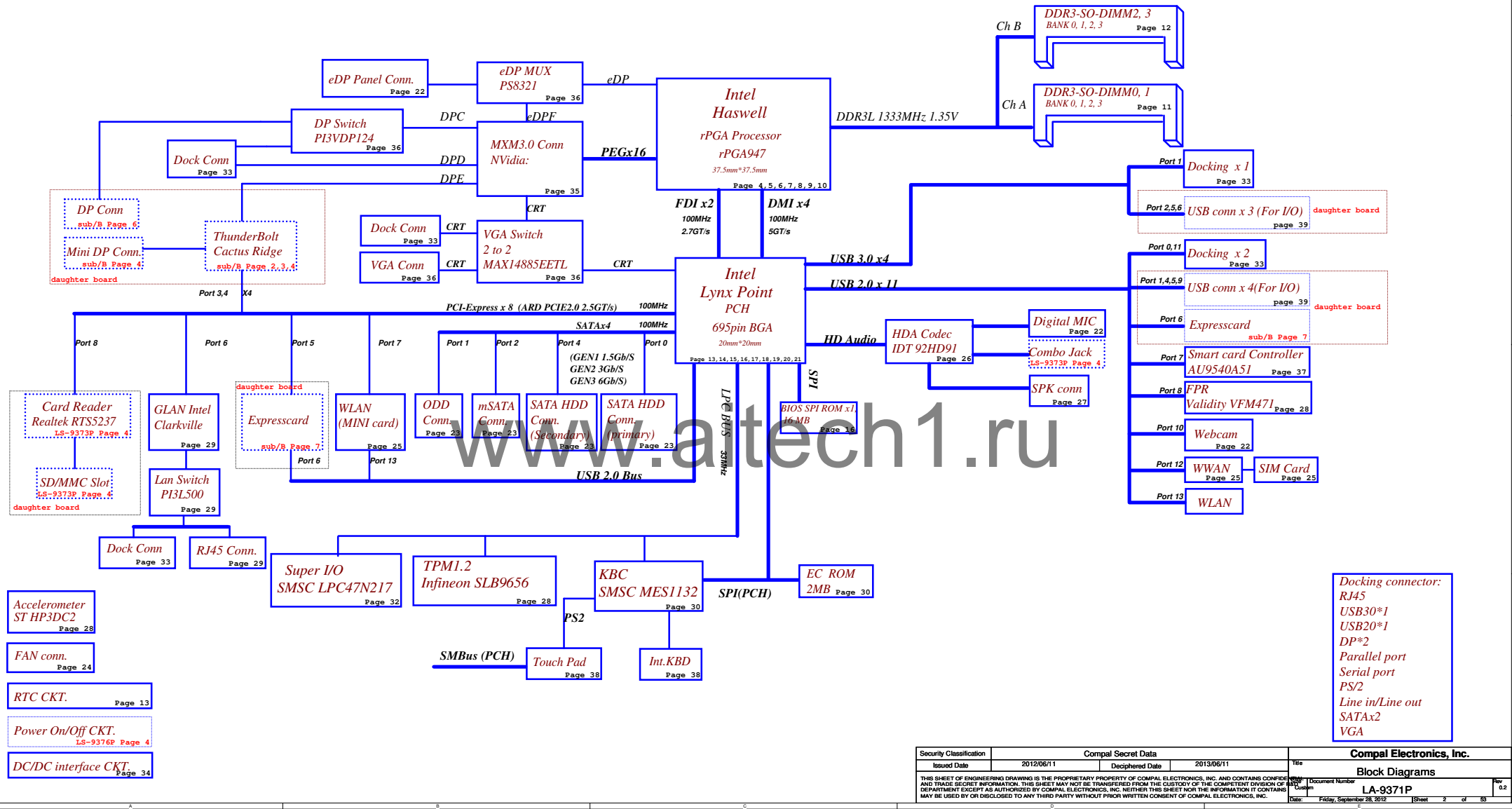
Afterburn MXM

LA-9371P

2012-09-28

REV : 0.2

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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	Cover Page
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Docking connector:  
RJ45  
USB30\*1  
USB20\*1  
DP\*2  
Parallel port  
Serial port  
PS/2  
Line in/Line out  
SATAx2  
VGA

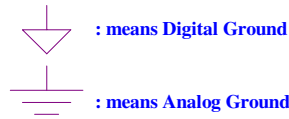
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## Voltage Rails

( O MEANS ON X MEANS OFF )

power plane State	+RTCVCC	B+	+5VDS +3VDS	+1.35V +0.675VS	+5VS +3VS +1.5VS +VCC_CORE +1.05VS +1.05VM	
S0	O	O	O	O	O	
S1	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

## Symbol Note :



@ : means just reserve , no build

AMT@ : means just install for support iAMT

CONN@ : means ME part.

Layout Notes

07/24 update

: Question Area Mark.(Wait check)

**Install below 45 level BOM structure for ver. 0.1**

45@ : means just put it in the BOM of 45 level.

**Install below 43 level BOM structure for ver. 0.1**

DEBUG@ : means just build when PCIE port 80 CARD function enable. Remove before MP

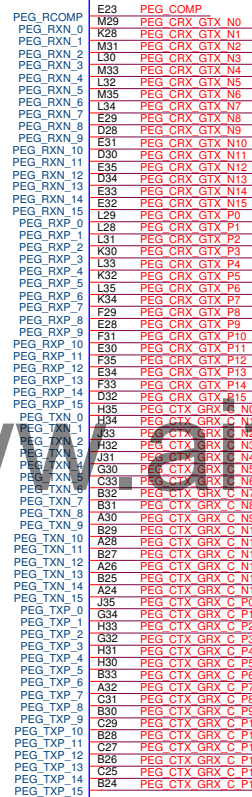
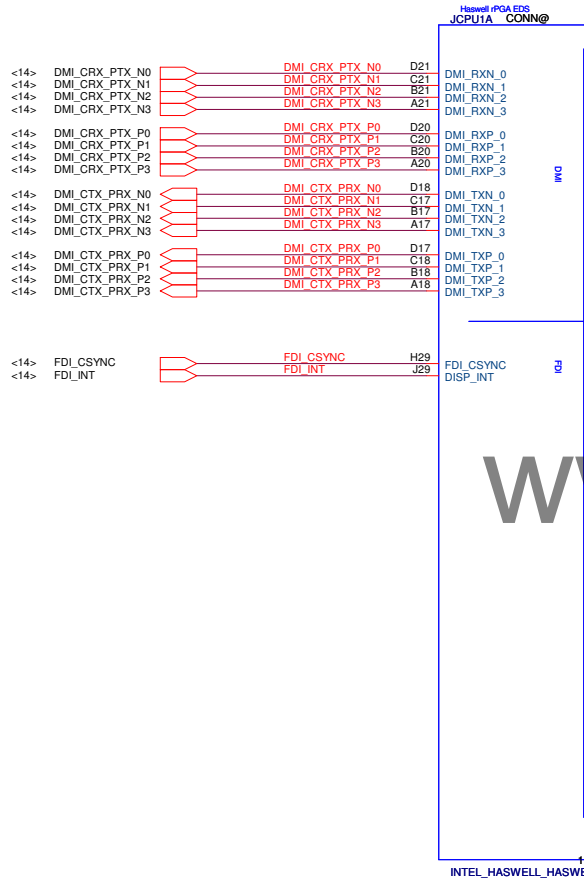
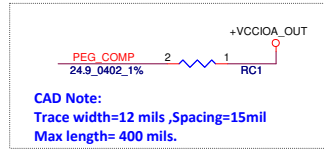
SMBUS Control Table

	SOURCE	BATT	2nd BATT	XDP	SODIMM	G-SENSOR	TP	NIC	NFC	EC	MXM
I2C_MAIN_CLK I2C_MAIN_DAT	SMSC1126	V	X	X	X	X	X	X	X	X	X
I2C_BAY_CLK I2C_BAY_DAT	SMSC1126	X	V	X	X	X	X	X	X	X	X
MEM_SMBCLK MEM_SMBDATA	Haswell	X	X	V	V	V	V	X	X	X	X
LAN_SMBCLK LAN_SMBDATA	Haswell	X	X	X	X	X	X	V	V	X	X
SML1_SMBCLK SML1_SMBDATA	Haswell	X	X	X	X	X	X	X	X	V	V

Stapping Options Flash

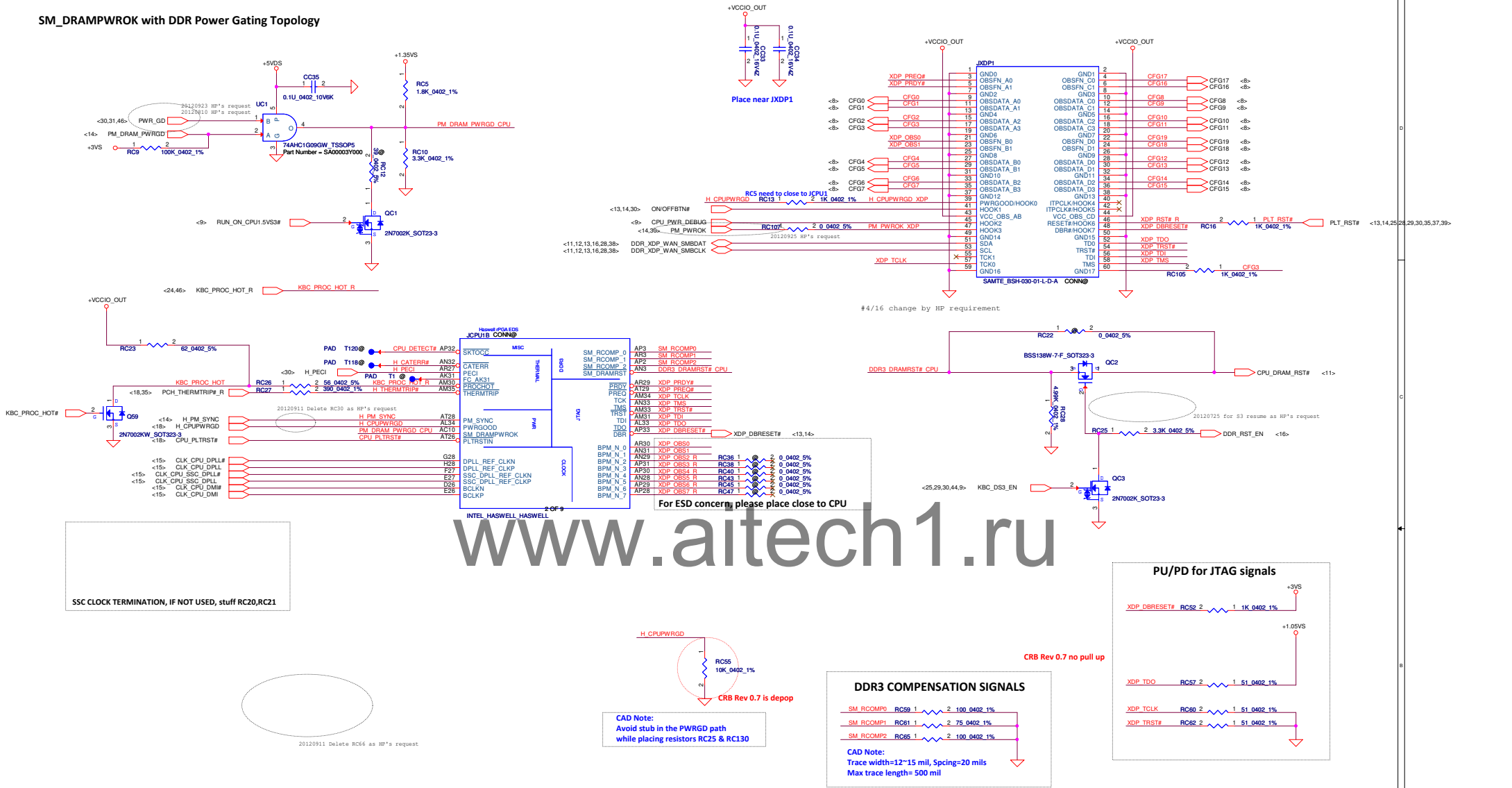
GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

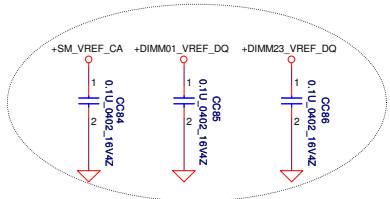
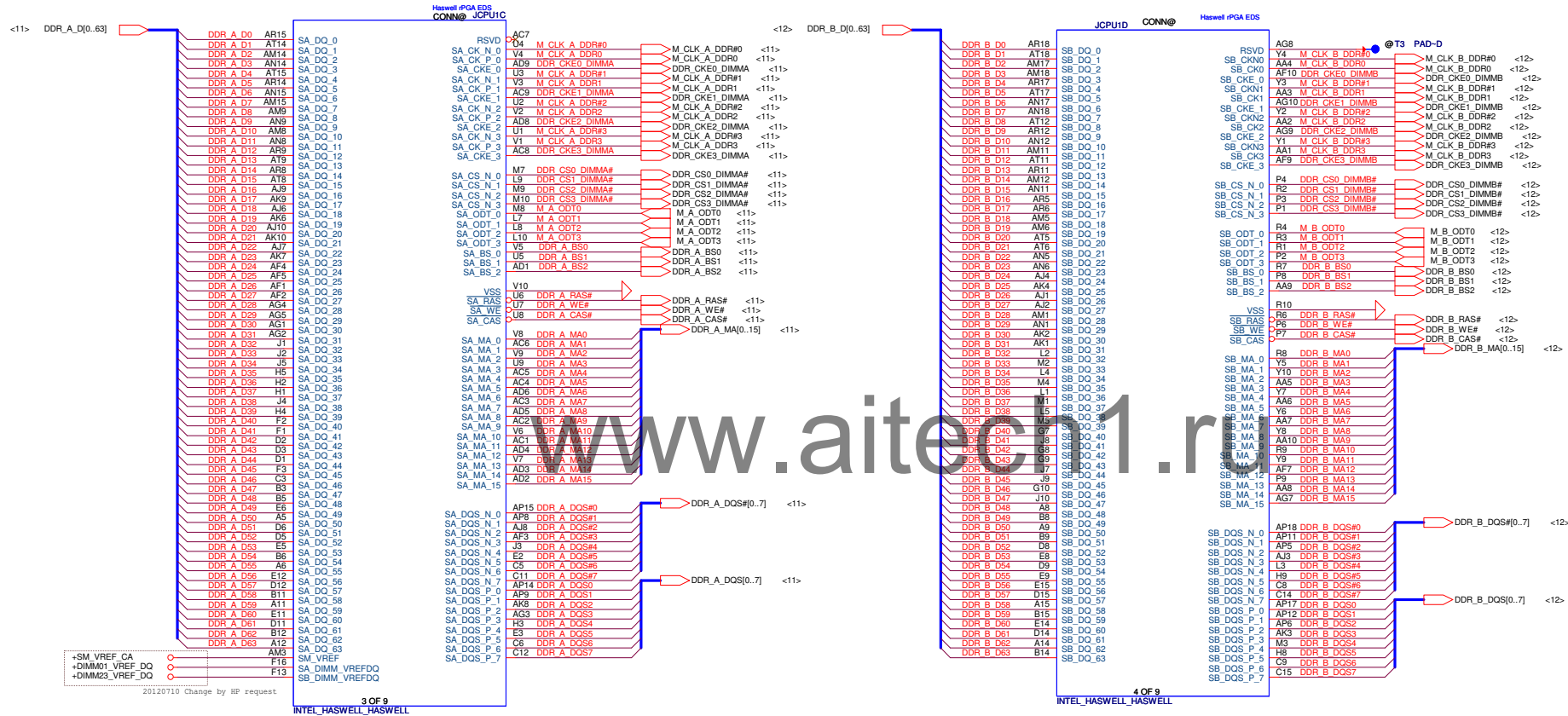
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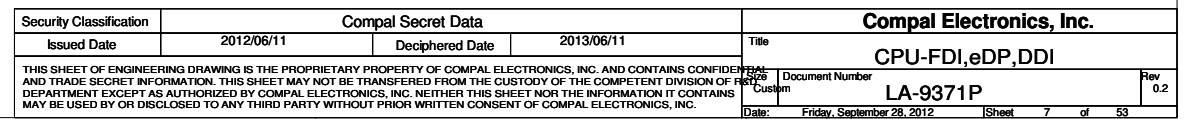
# SM\_DRAMPWROK with DDR Power Gating Topology



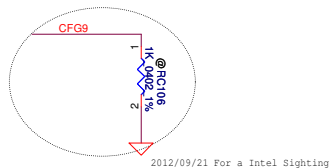
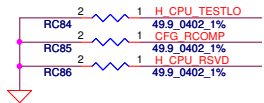


**Layout Notes**  
Place C84,C85,C86 close to JCPU1

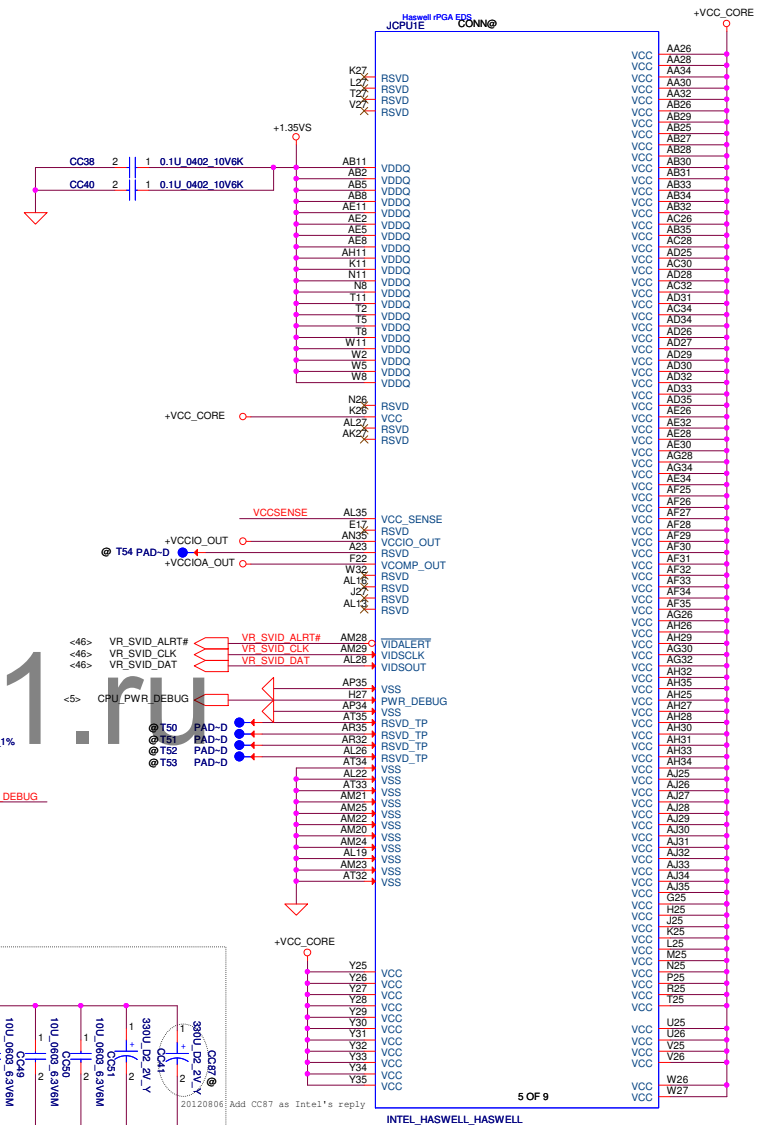
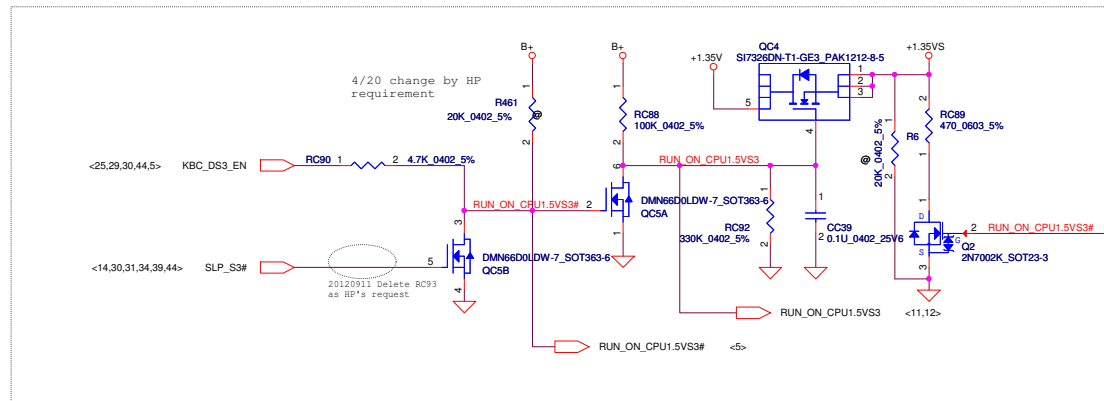
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A circuit diagram showing a 1k resistor (1K 0402 1%) connected to a CF7 signal source and ground. The resistor is represented by a zigzag line with the value '1K 0402 1%' written next to it. One end of the resistor is connected to a line labeled 'CF7'. The other end is connected to a ground symbol, which is a triangle pointing downwards.

[illegible]

### +1.35VS Source

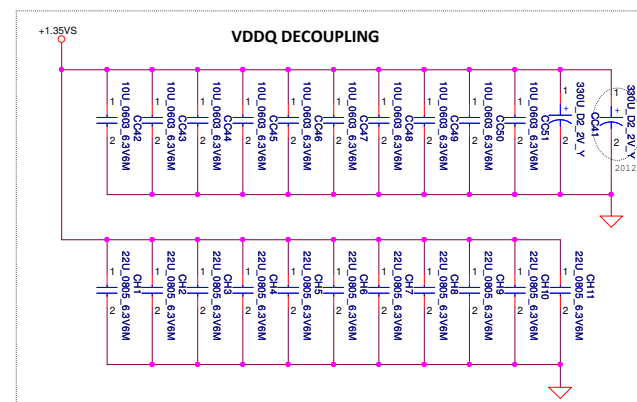
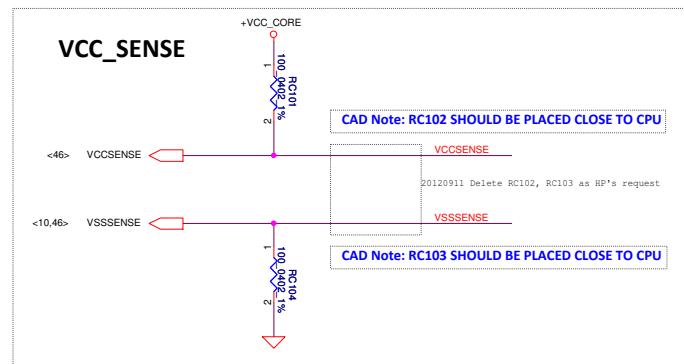


## SVID ALERT

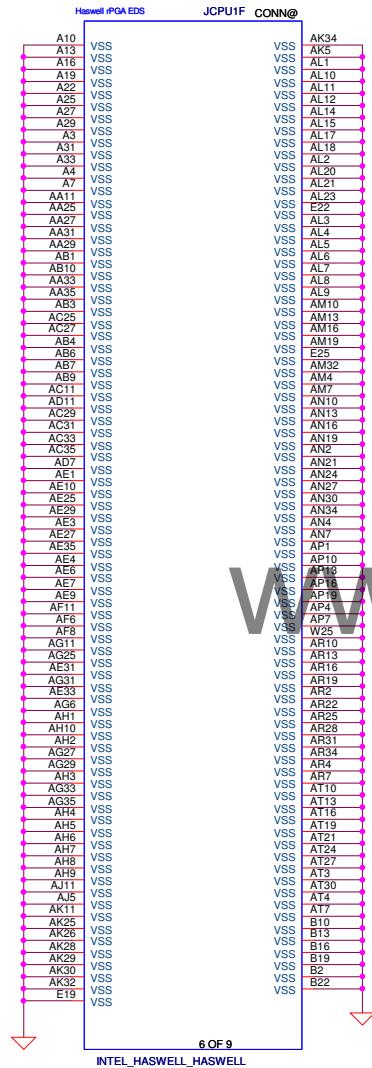
**CAD Note: Place the PU resistors close to CPU  
RC60 close to CPU 300 - 1500mils**

## SVID DATA

**CAD Note: Place the PU resistors close to CPU  
RC63 close to CPU 300 - 1500mils**



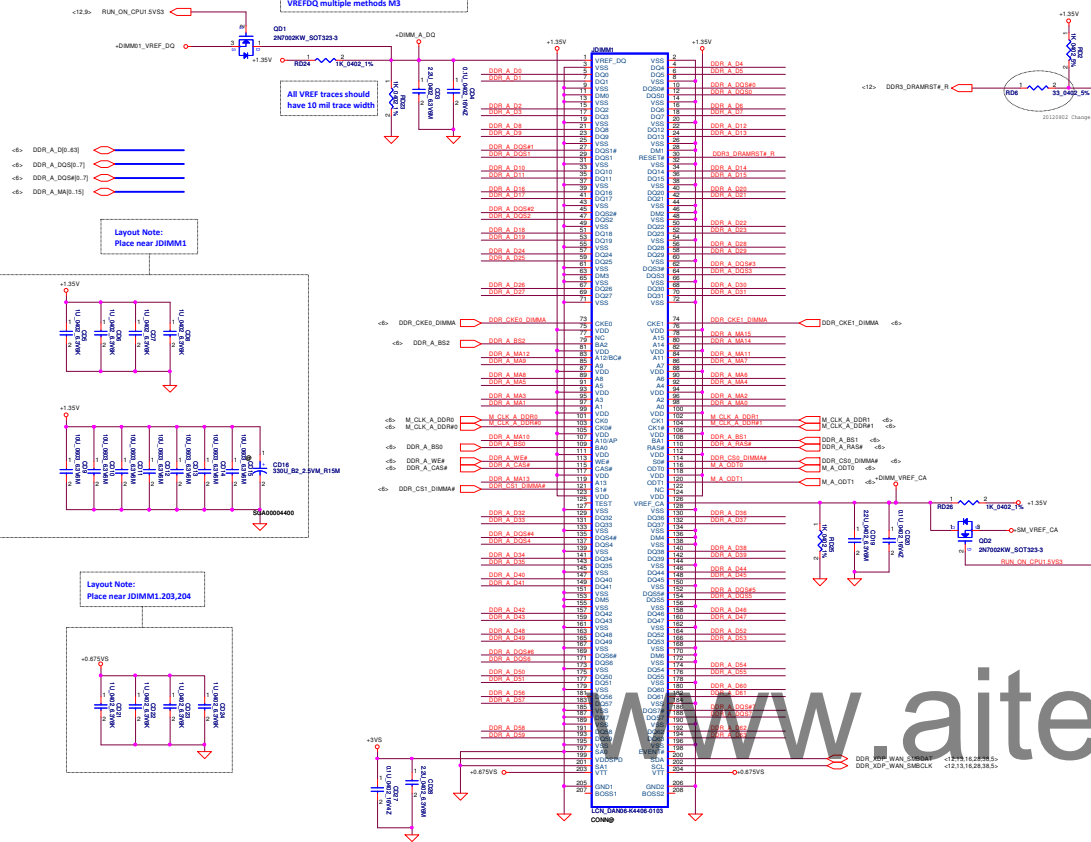
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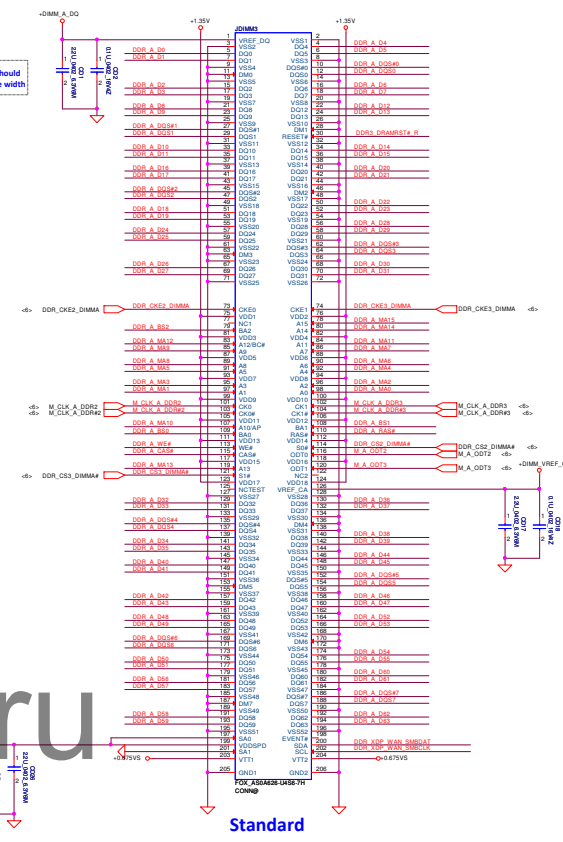
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## JDIMM3 H=4.0mm BOT

## JDIMM1 H=5.2 mm TOP



Reverse



## Standard

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			Compul	Issue	11 of 53

## JDIMM4 H=4.0mm BOT

<6> DDR\_B\_D[0..63]

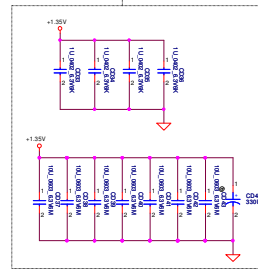
<6> DDR\_B\_DQS[0..7]

<6> DDR\_B\_DQS# [0..7]

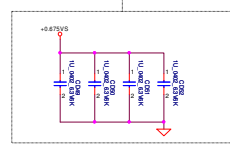
<6> DDR\_B\_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note:  
Place near JDIMM2



Layout Note:  
Place near JDIM

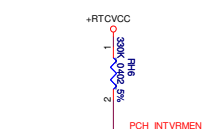


Reverse

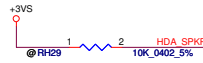
Reverse

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INTVRMEN - INTEGRATED SUS 1.05V VRM  
ENABLE  
High - Enable Internal VRs  
Low - Enable External VRs



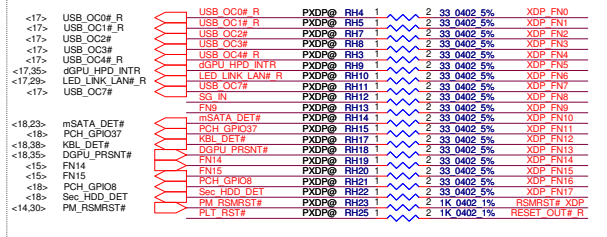
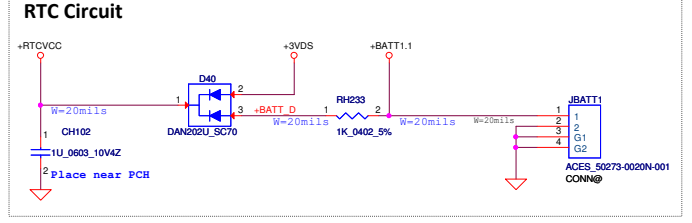
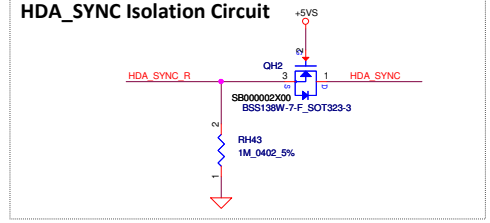
NO REBOOT STRAP  
DISABLED WHEN LOW (DEFAULT)  
ENABLED WHEN HIGH



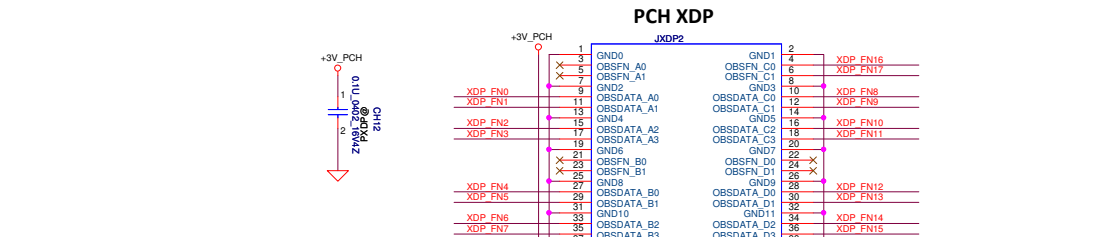
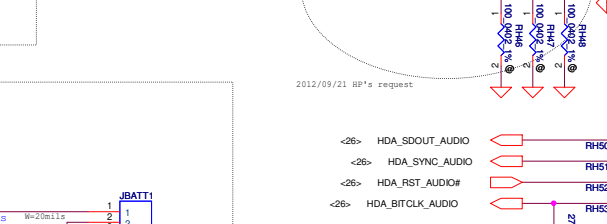
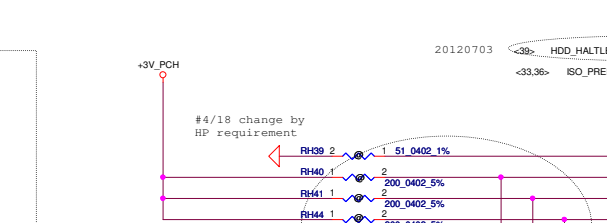
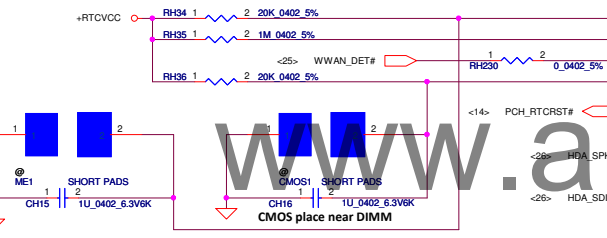
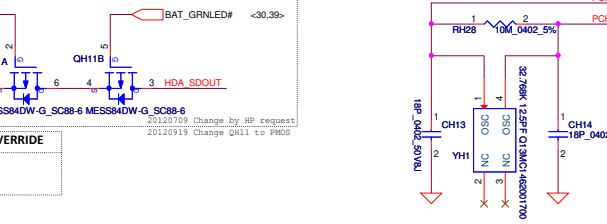
20120802 HP's request

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

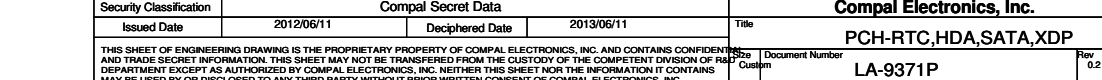
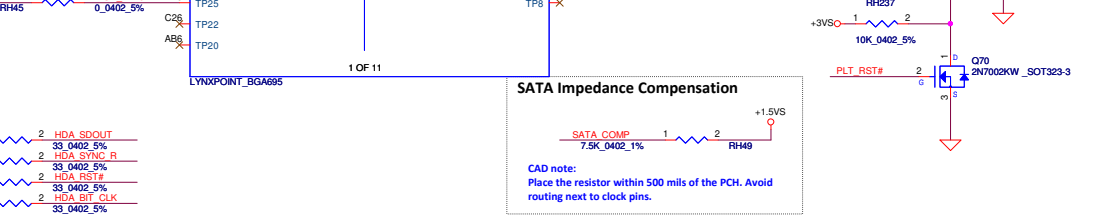
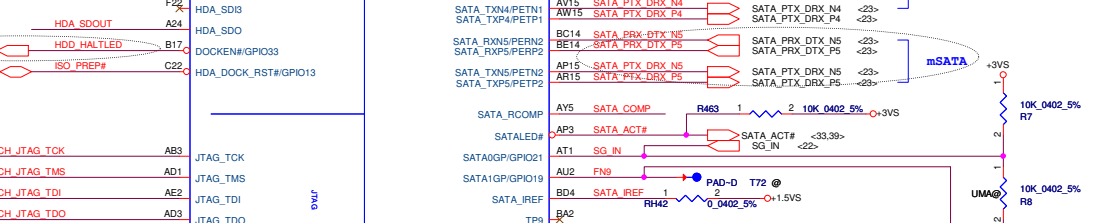
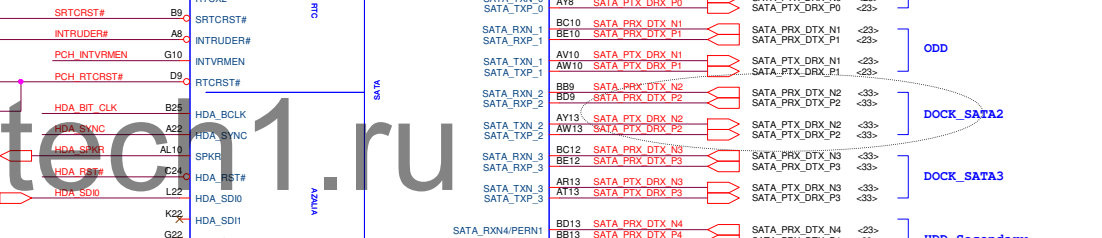
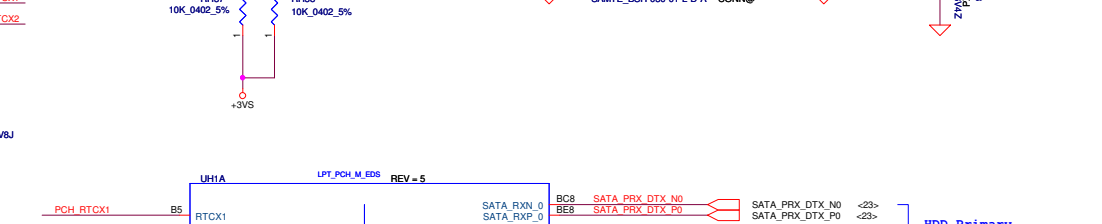
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



#4/18 change by HP requirement



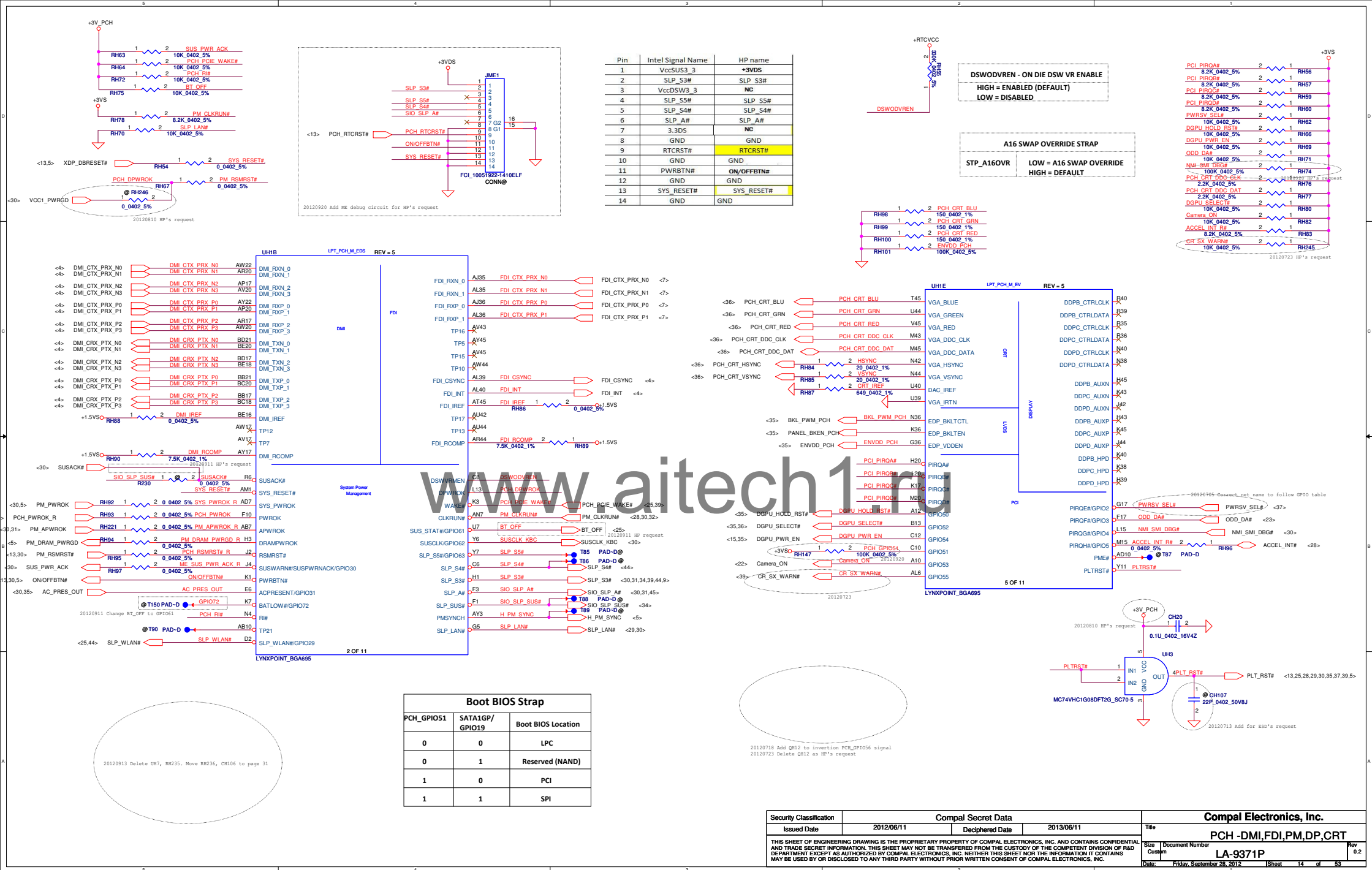
#4/18 change by HP requirement



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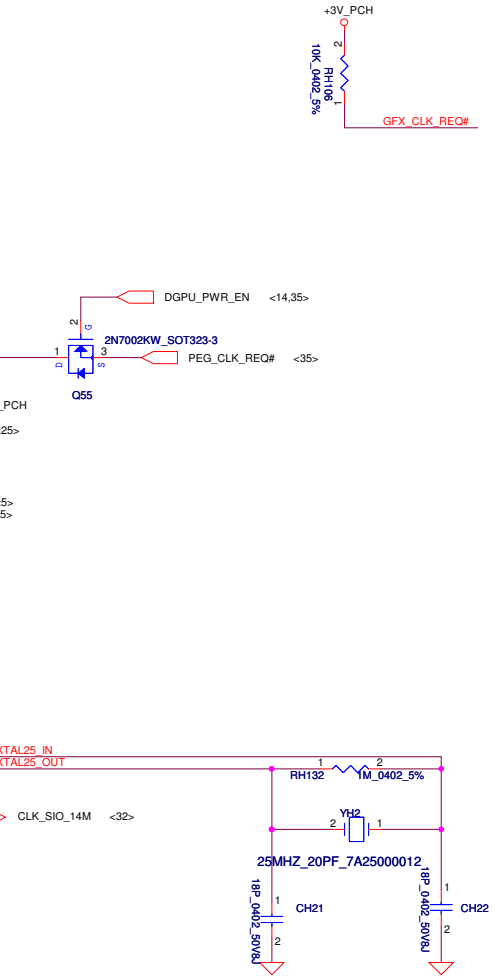
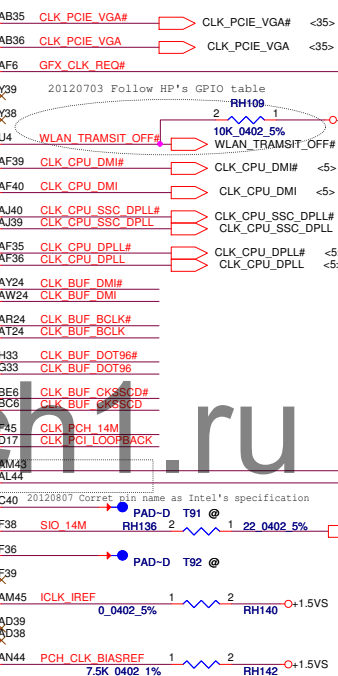
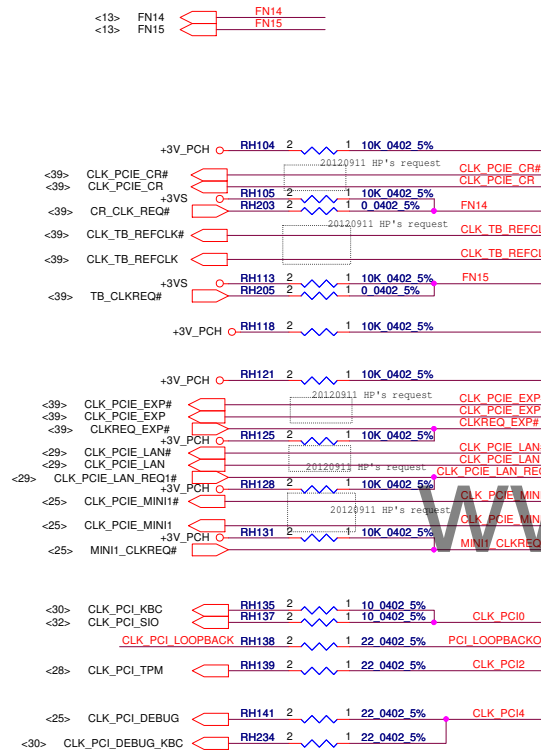
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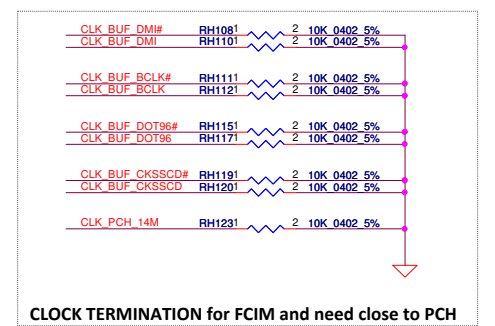


Boot BIOS Strap		
PCH_GPIOS1	SATA1GP/ GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

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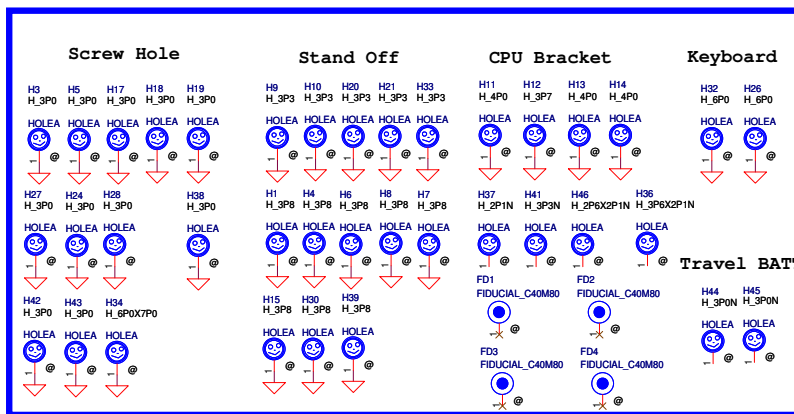
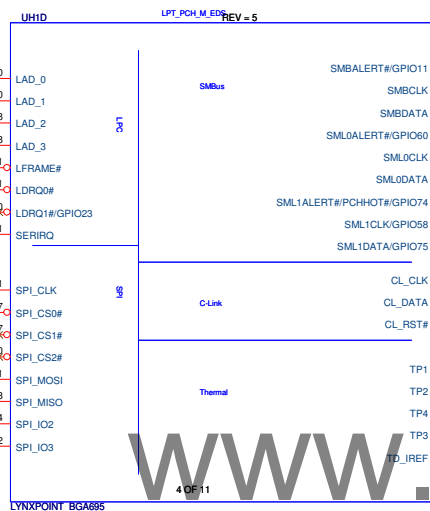


PCIECLK REQ Pull UP Power Rail:  
SUS Rail : 0 3 4 5 6 7  
Core Rail: 1 2



CLOCK TERMINATION for FCIM and need close to PCH

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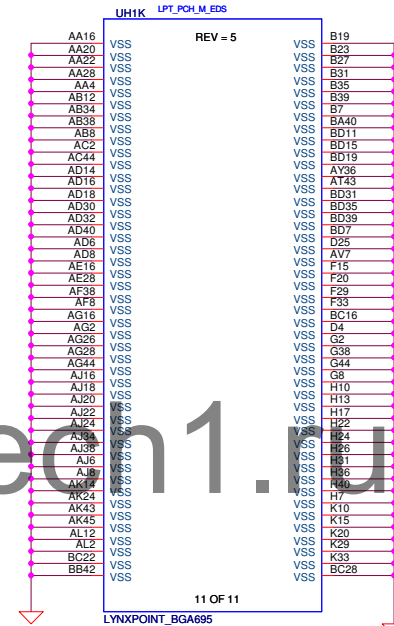
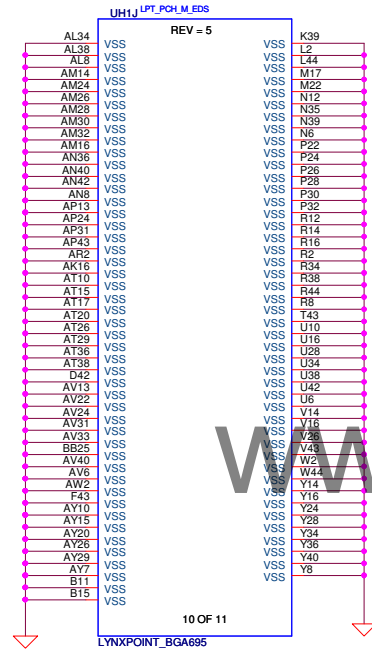






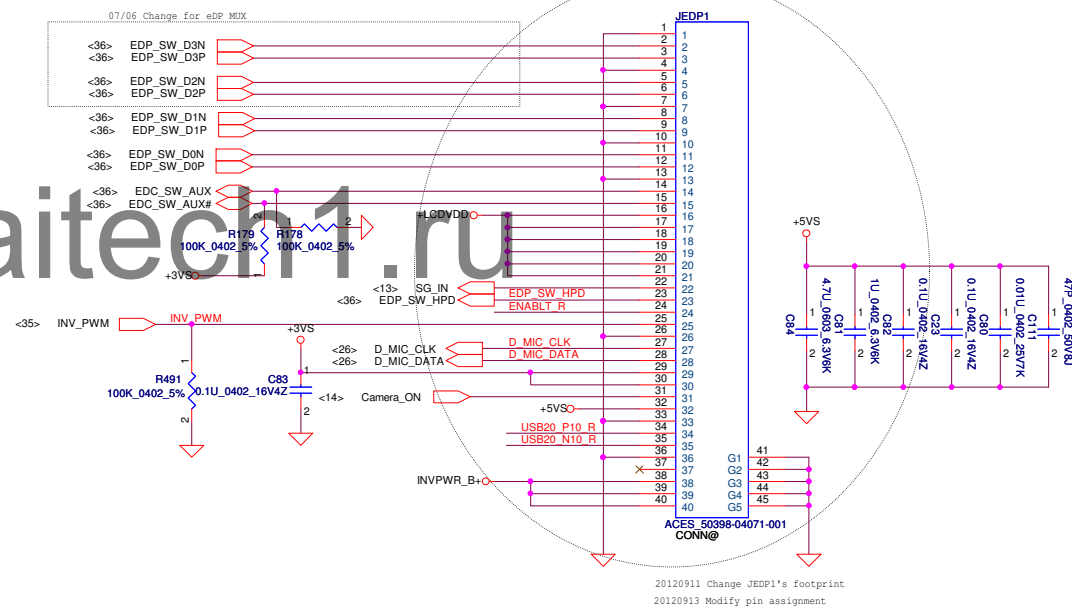
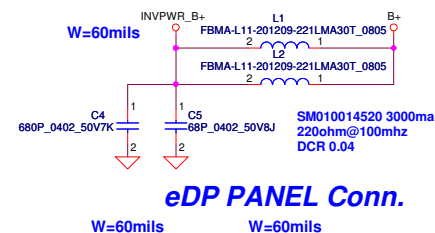
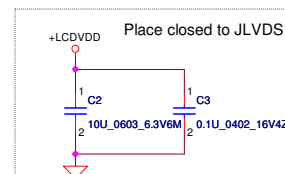
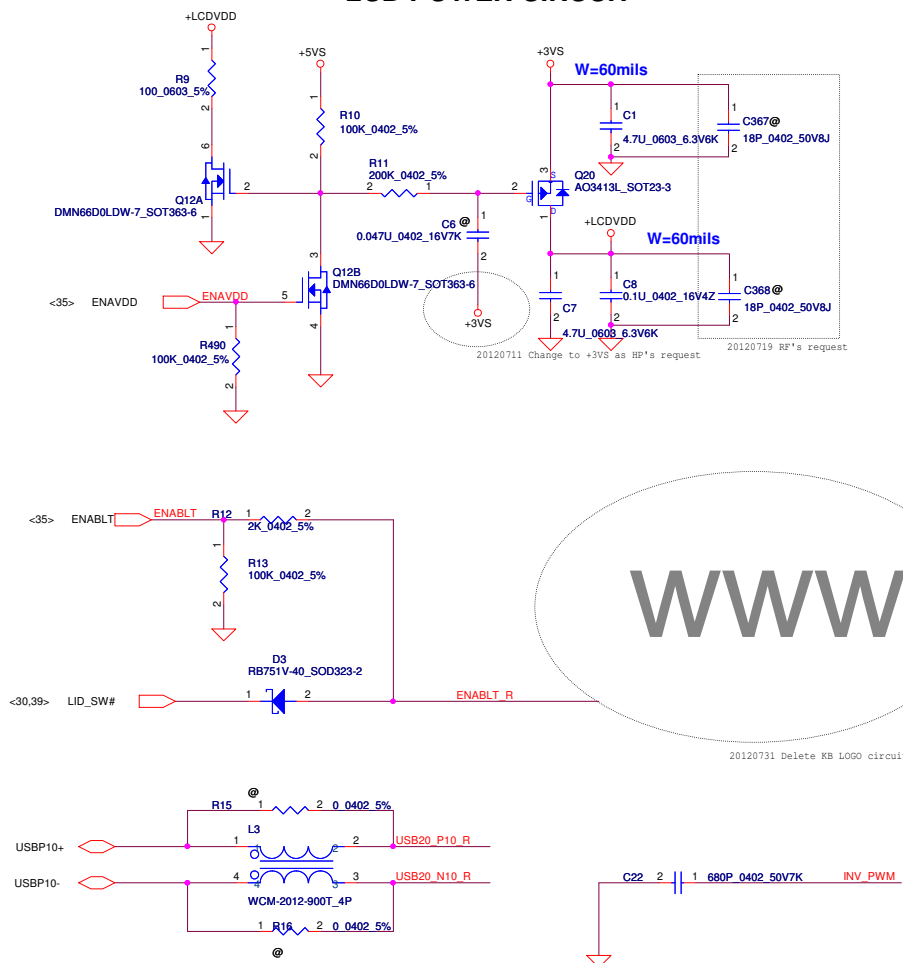






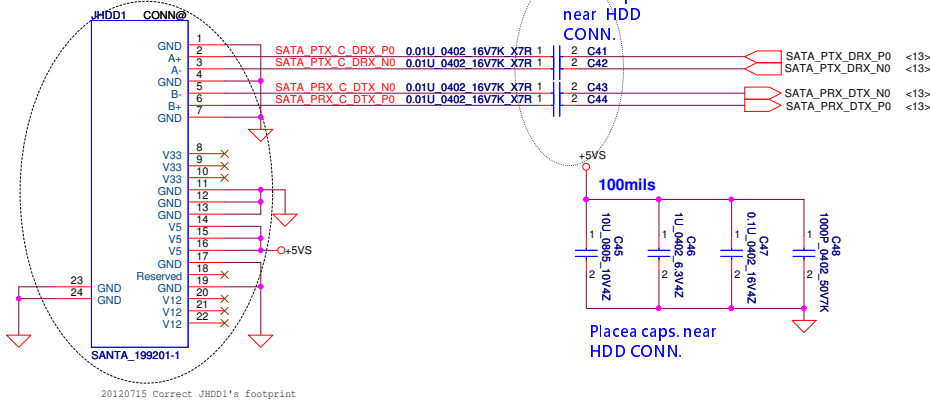
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						Document Number	LA-9371P		Rev	0.2
						Date:	Friday, September 28, 2012		Sheet	21 of 53

## LCD POWER CIRCUIT

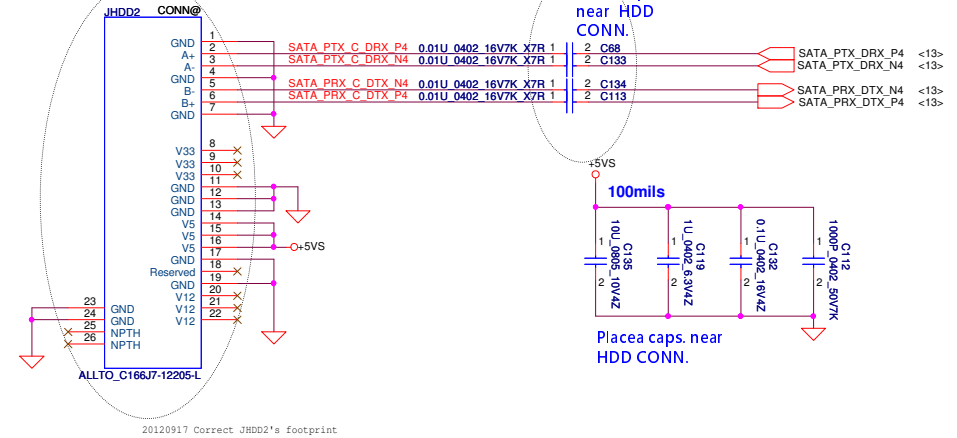


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				Document Number	LA-9371P
				Date:	Friday, September 28, 2012
				Sheet	22 of 53
				Rev	0.2

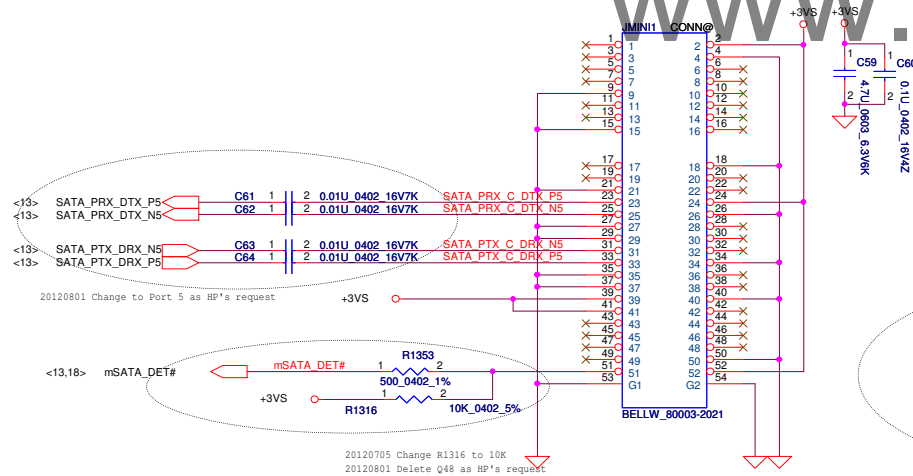
## SATA Primary HDD CONN.



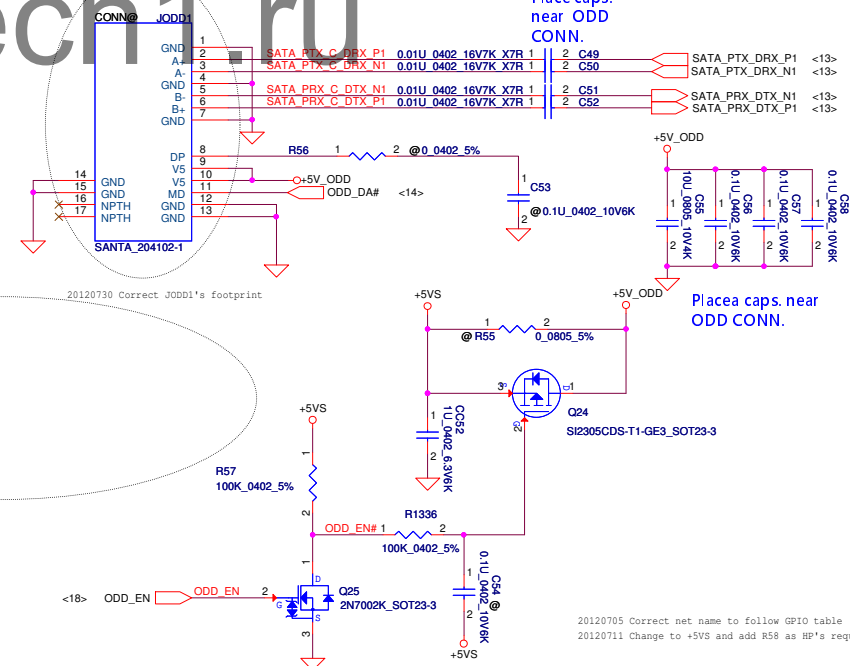
## SATA Second HDD CONN.



## mSATA Conn.

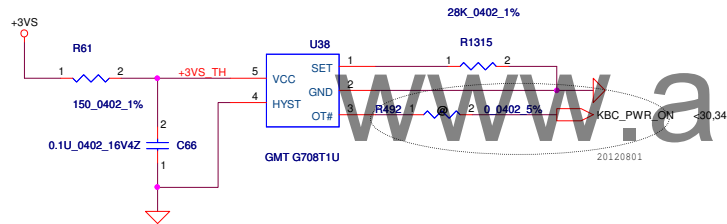
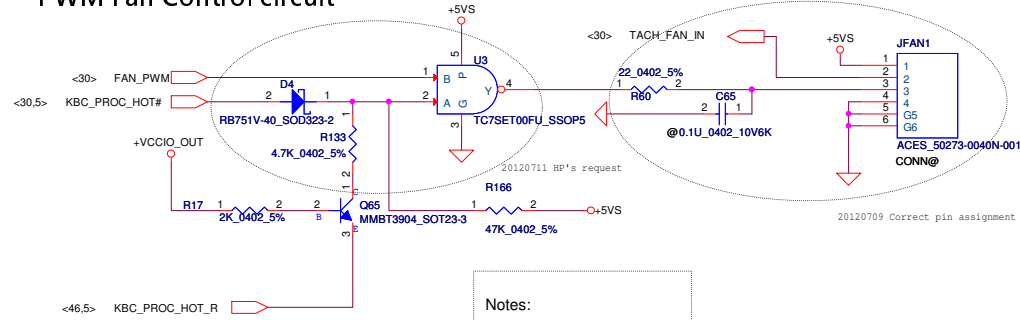


## SATA ODD CONN.



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				Date:	Friday, September 28, 2012
				Sheet	23 of 53

## PWM Fan Control circuit



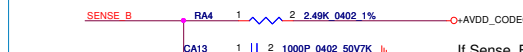
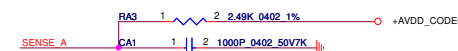
Security Classification	Compal Secret Data			Title	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Sandy(2/7) PM,XDP,Thermal	
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				LA-9371P	0.2
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Notes:  
Keep PVDD supply and speaker traces routed on the DGND plane.  
Keep away from AGND and other analog signals

PLACE CLOSE TO U1 PIN 13

If Sense\_A total length is greater than 6 inches, change C12 to 0.1uF



PLACE CLOSE TO U1 PIN 14

If Sense\_B is un-used, then pull high Sense\_B to AVDD by 10Kohm resistor

External MIC  
Combo Jack  
Headphone

Internal SPKR(front stereo speaker)

20120702 Delete MIC\_SENSE# circuit

20120702 Delete MUTE circuit

Place C209,C210,CA87,CA89 close to Codec

GND

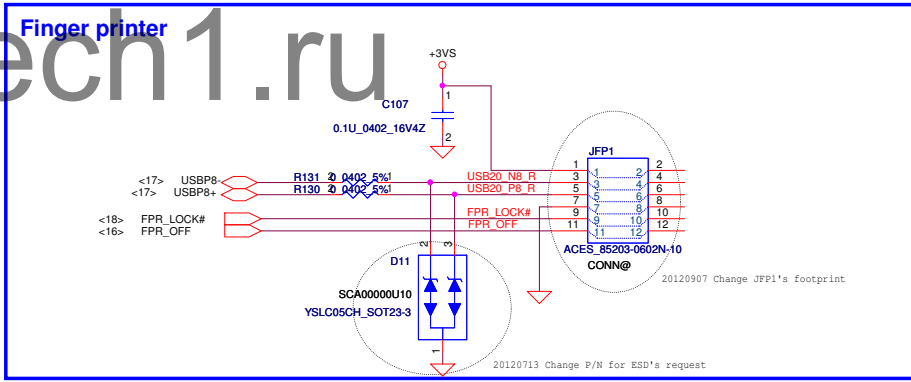
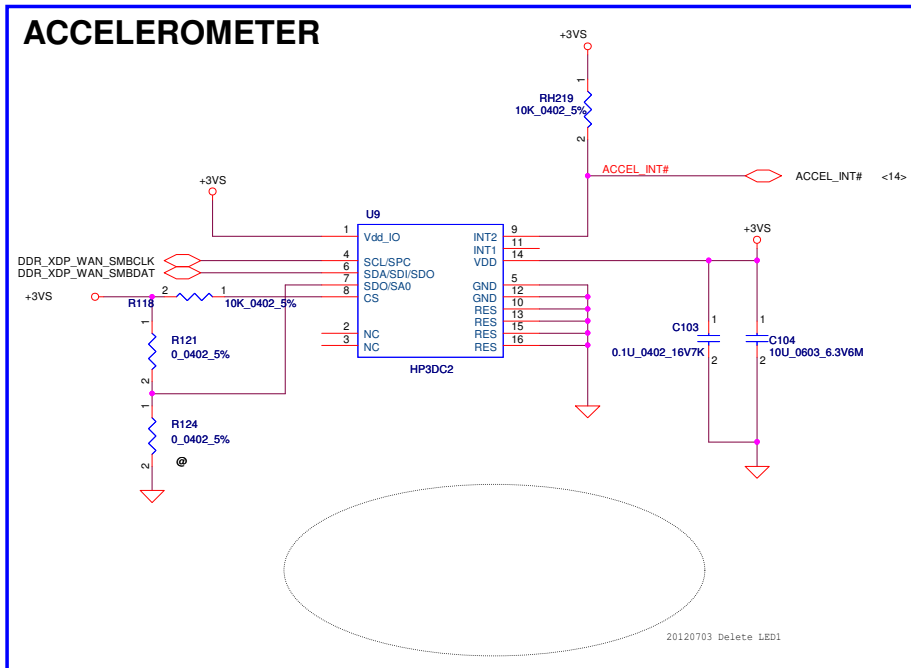
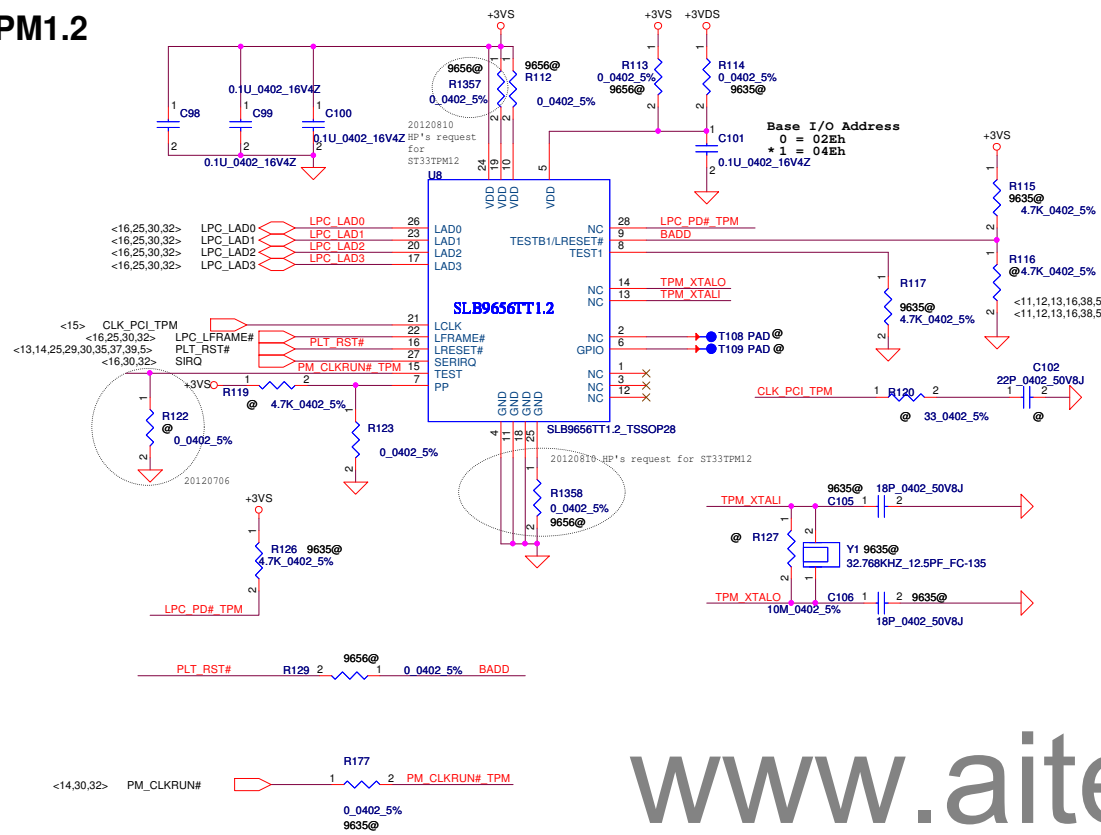
GNDA

RA53 need under or near UA1

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				Customer	LA-XXXXP
				Date	Friday, September 28, 2012
				Sheet	26 of 53



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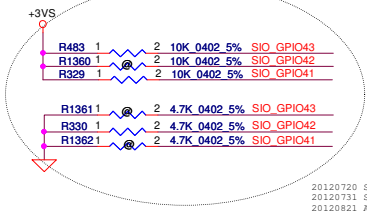
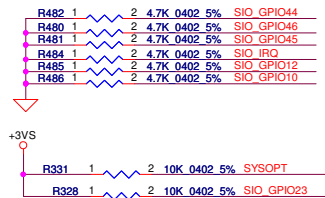
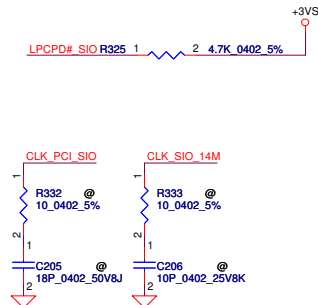
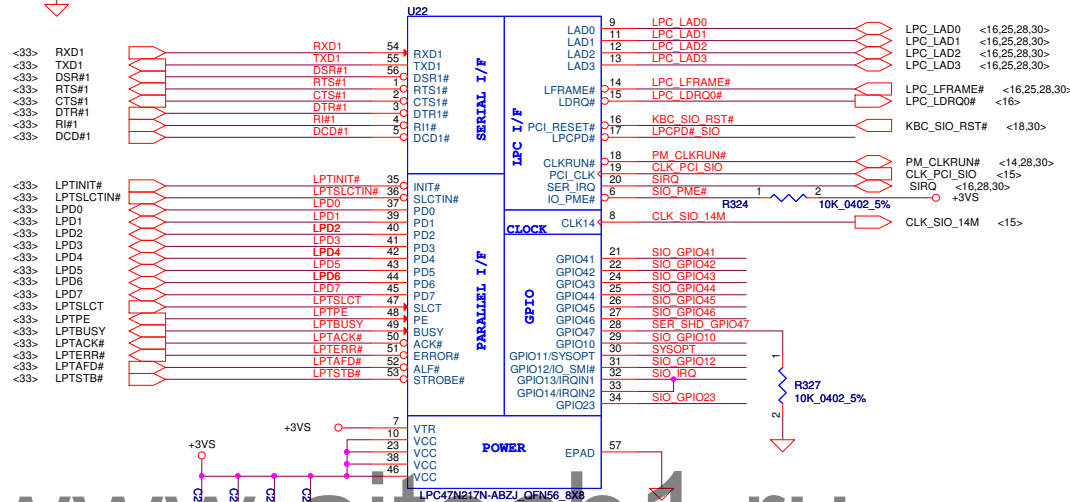
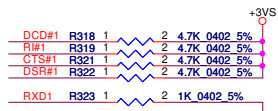
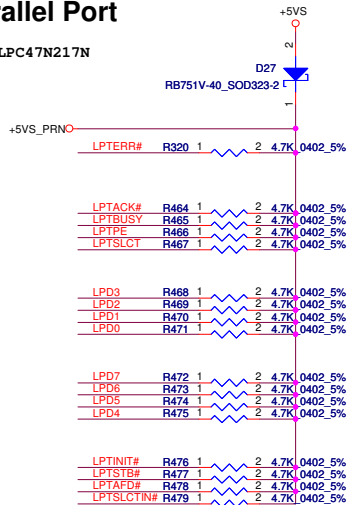






## Parallel Port

TO LPC47N217N



20120720 System ID for HP's request  
20120731 System ID for HP's request  
20120821 Add R for 2019M & 4019M option

## Platform IDs (Super I/O GPIOs)

PLT_ID1	PLT_ID2	PLT_ID3	SYSTEM ID	Series	CPU	Dock	COMMON BIOS
GPIO43	GPIO42	GPIO41	Afterburner 17" 4 DIMM	W	Haswell	Common	8
1	0	1	Afterburner 17" 2 DIMM	W	Haswell	Common	8
1	1	1					

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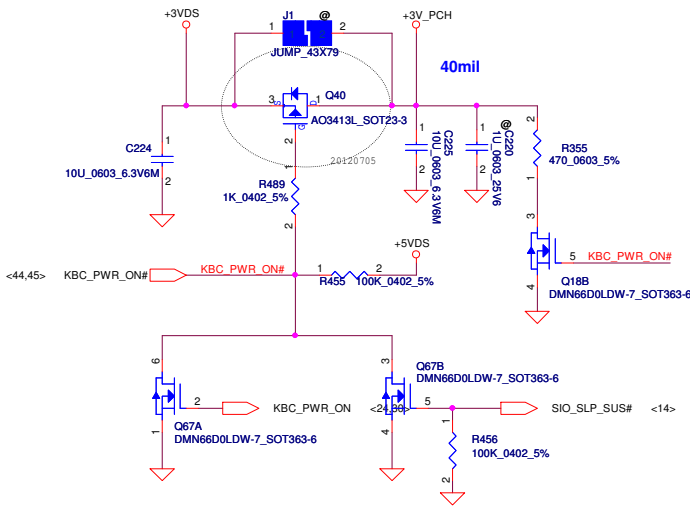
## ***DOCKING CONNECT***



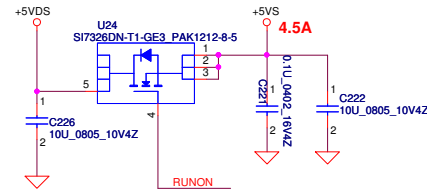
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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	
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				Custom	LA-9371P
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### +3VALW TO +3VALW(PCH AUX Power)

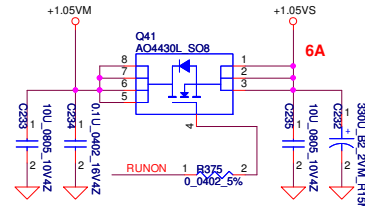
Short J1 for PCH VCCSUS3.3



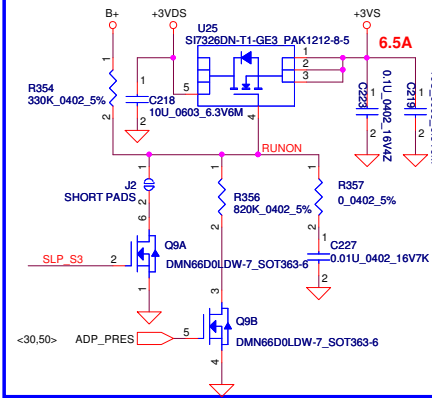
### +5VALW to +5VS Transfer



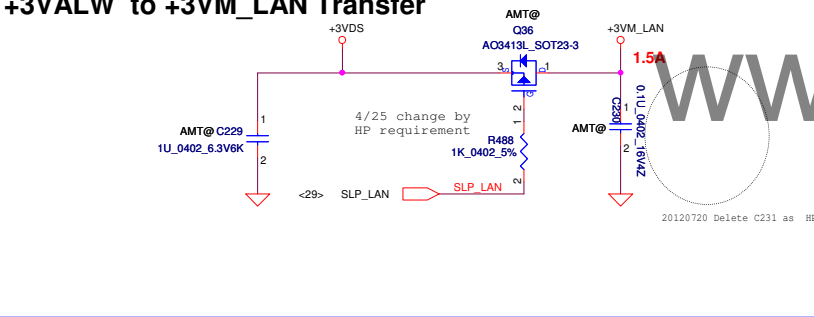
### +1.05VM to +1.05VS Transfer



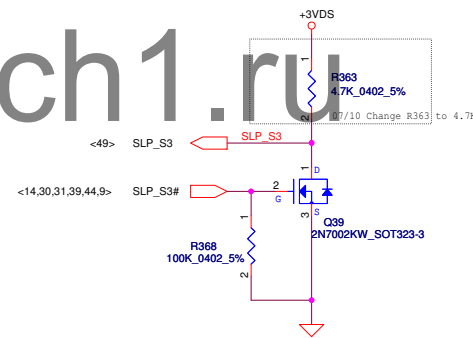
### +3VALW to +3VS Transfer



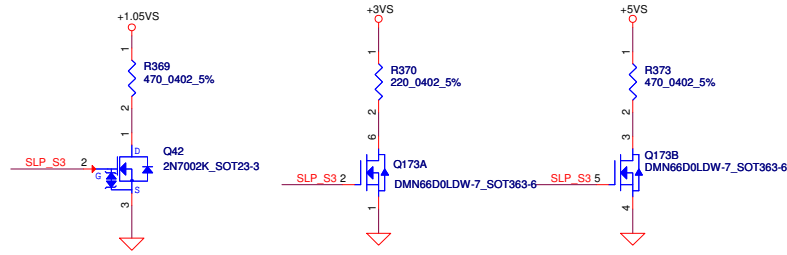
### +3VALW to +3VM\_LAN Transfer



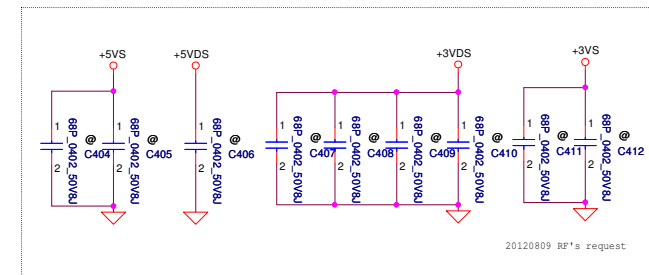
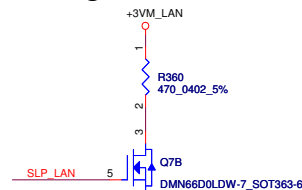
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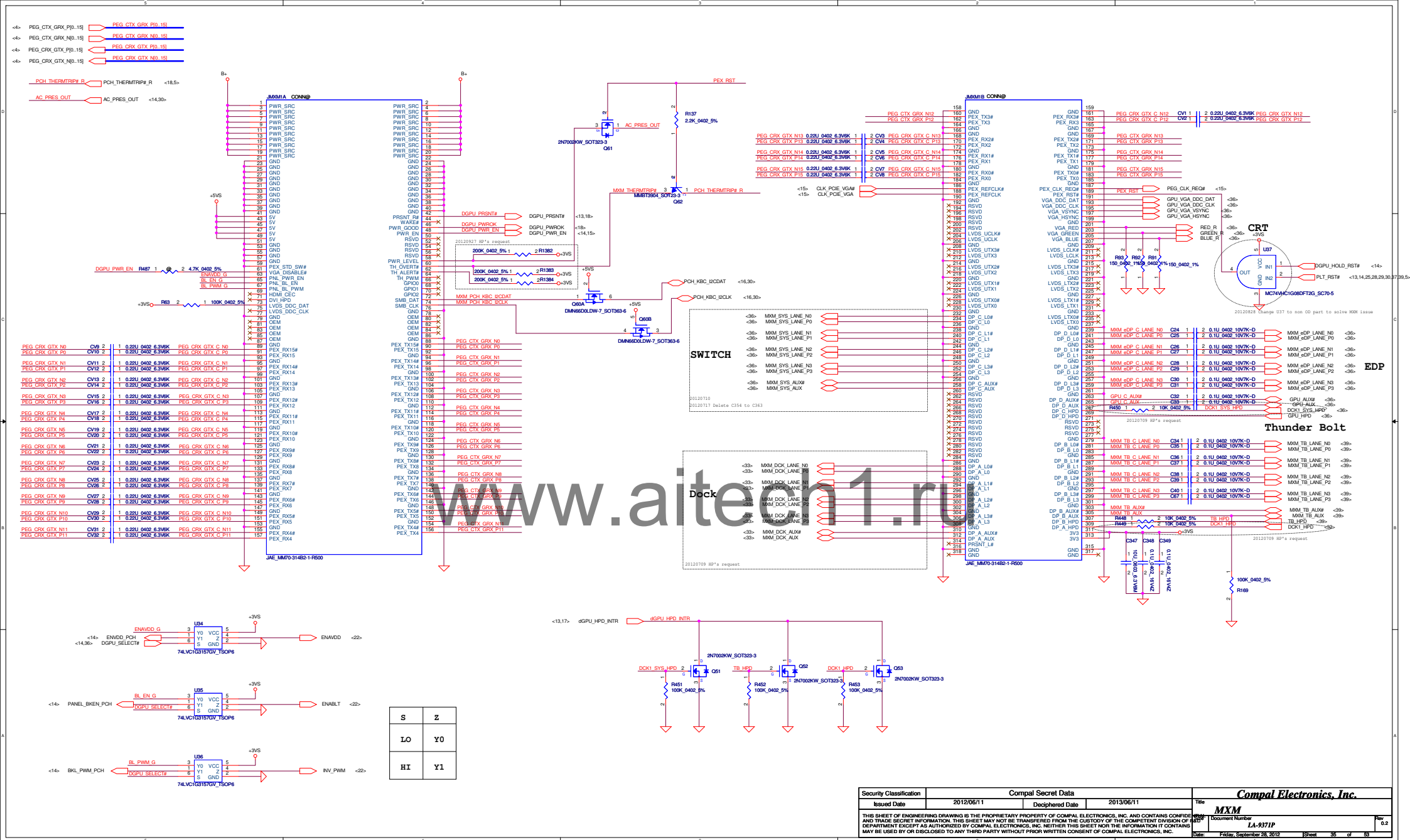
### Discharge circuit-1



### Discharge circuit-2 for V-M

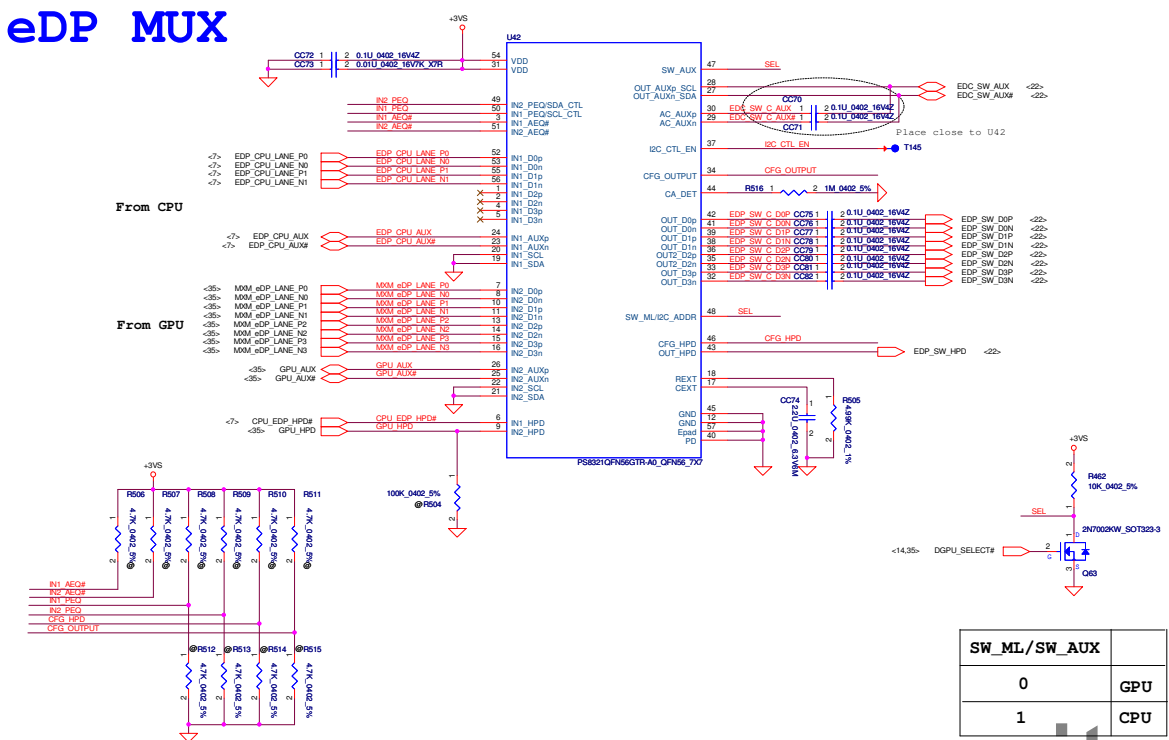




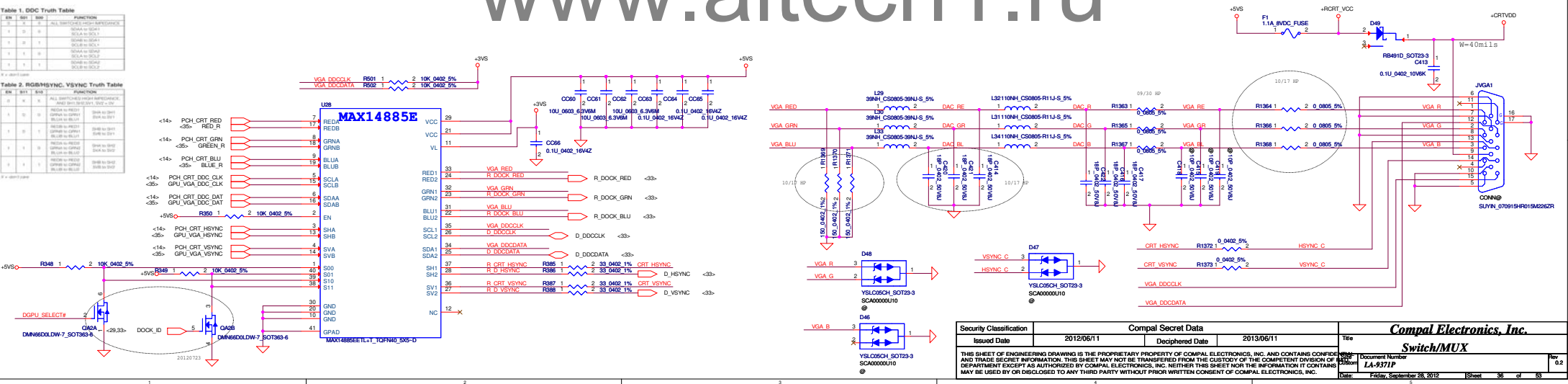
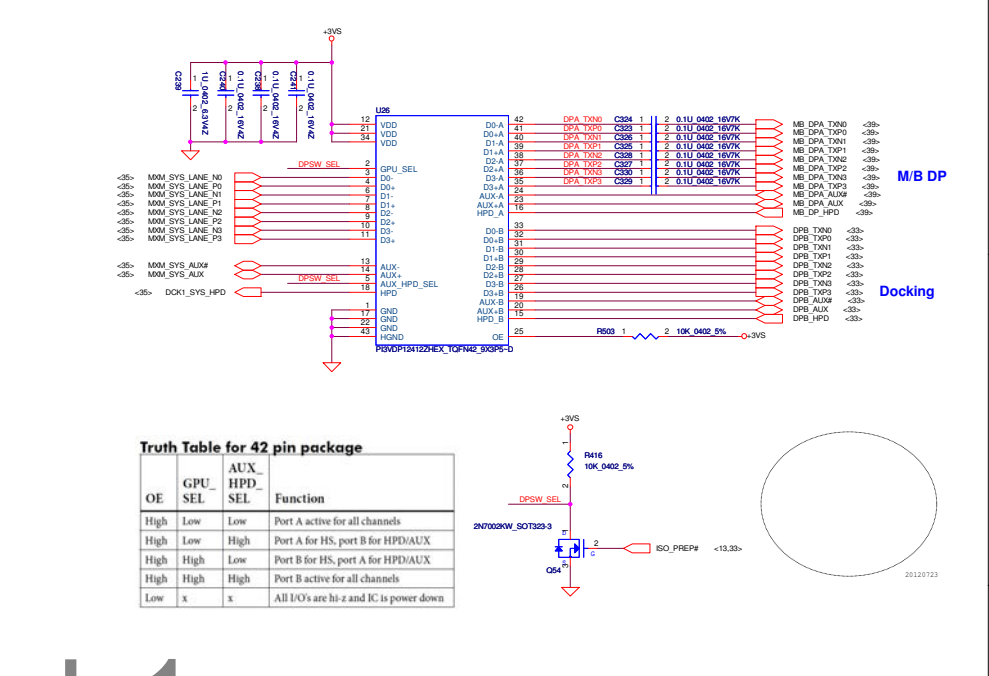


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				Project Number		
				LA-937IP		
Date:	Fri Jun 8, September 26, 2012	Sheet	35	of	53	Pov 0.2

# eDP MUX

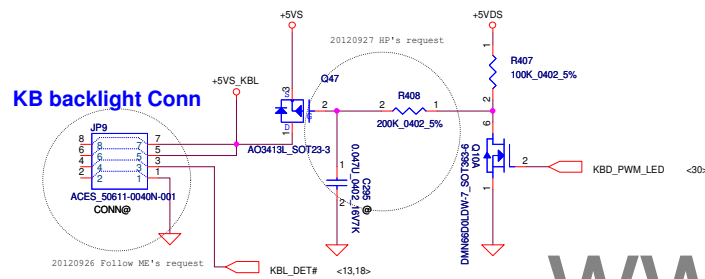
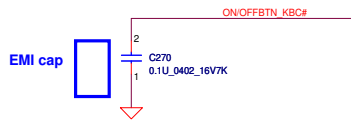
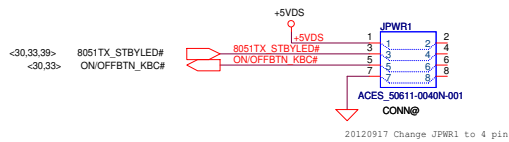


# DP Switch

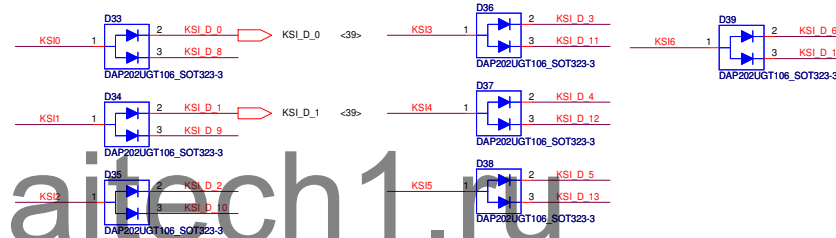
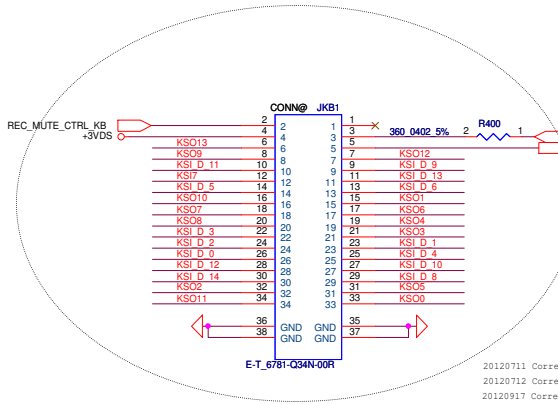
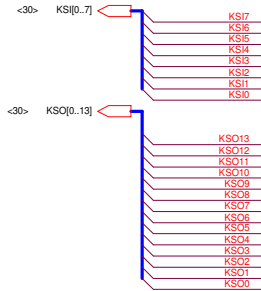
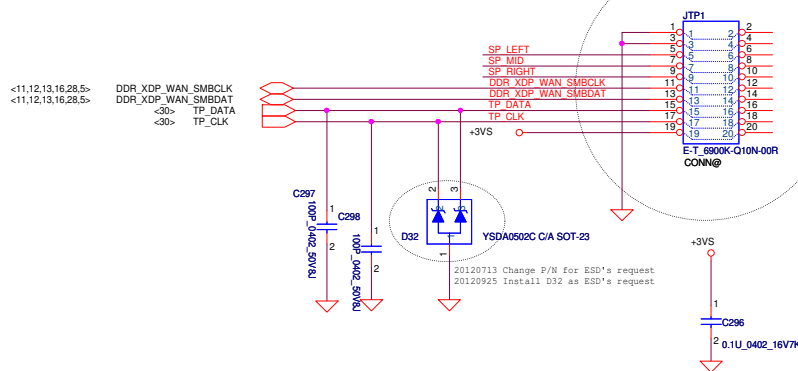




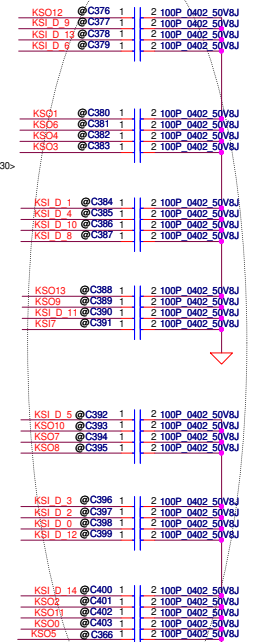
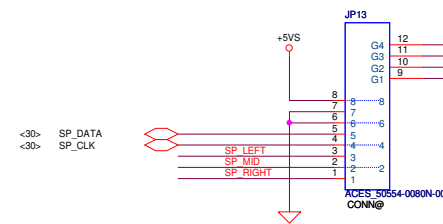




# TP/B TO M/B



# Stick Point CONN



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Size		Document Number		Rev	
Cuskm		1		0.2	
Date		Friday, September 28, 2012		Sheet	
		38		of	
		53			

Pinout diagram for the E-T 6800K-Q10N-00R connector. The diagram shows a 20-pin connector with pins numbered 1 to 20. The pins are connected to various components: +5V, +3VDS, KSI\_D\_0, KSI\_D\_1, KSOI7, MUTE\_LED\_CNTR, MUTE\_LED\_CNTR, LID\_SW#, and LID\_SW#. The diagram also shows the correct footprint for the connector, with pins 1 to 20 labeled. The diagram is titled 'E-T 6800K-Q10N-00R CONN@'.

Pin	Signal
1	+5V
2	+3VDS
3	KSI_D_0
4	KSI_D_1
5	KSOI7
6	MUTE_LED_CNTR
7	MUTE_LED_CNTR
8	LID_SW#
9	LID_SW#
10	LID_SW#
11	LID_SW#
12	LID_SW#
13	LID_SW#
14	LID_SW#
15	LID_SW#
16	LID_SW#
17	LID_SW#
18	LID_SW#
19	LID_SW#
20	LID_SW#

E-T 6800K-Q10N-00R CONN@

20120715 Correct JFB1's footprint  
 20120812 Correct JFB1's footprint & Pin assignment

The diagram illustrates the pin connections for the ACES\_50121-06001-001 connector. It shows a 60-pin connector with various signal lines and power planes.

**Power and Ground Connections:**

- +5VDS:** Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
- +3VS:** Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
- +5VDS +3VDS:** Connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60.
- GND:** Connected to pins 61, 62, 63, 64, 65, 66.

**Signal Connections:**

- USB:**
  - USB3TN5 (Pin 1)
  - USB3TP5 (Pin 2)
  - USB3RN5 (Pin 3)
  - USB3RP5 (Pin 4)
  - USBP4- (Pin 5)
  - USBP4+ (Pin 6)
  - USB3TN2 (Pin 7)
  - USB3TP2 (Pin 8)
  - USB3RN2 (Pin 9)
  - USB3RP2 (Pin 10)
  - USBP1- (Pin 11)
  - USBP1+ (Pin 12)
- PCIe:**
  - PCIE\_PTX\_C\_DRX\_P8 (Pin 13)
  - PCIE\_PTX\_C\_DRX\_N8 (Pin 14)
  - PCIE\_PRX\_DTX\_P8 (Pin 15)
  - PCIE\_PRX\_DTX\_N8 (Pin 16)
  - CLK\_PCIE\_CR (Pin 17)
  - CLK\_PCIE\_CR# (Pin 18)
  - CR\_CLK\_REQ# (Pin 19)
  - EXT\_MIC\_LF (Pin 20)
  - HP\_OUT\_R (Pin 21)
  - HP\_OUT\_L (Pin 22)
  - PCH\_PCIE\_WAKE# (Pin 23)
- HP Sense:**
  - HP\_SENSE# (Pin 24)
  - EN\_P1VS (Pin 25)
- Other:**
  - PLT\_RST# (Pin 26)
  - R1390 (Pin 27)
  - 0.0402 5% (Pin 28)

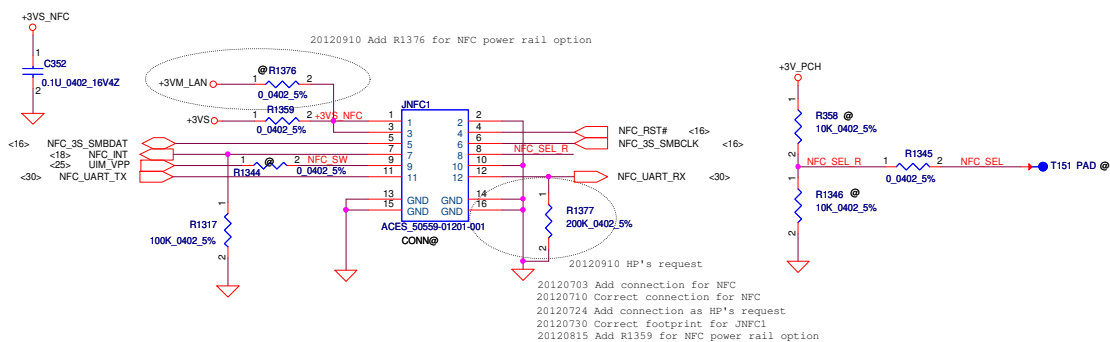
The diagram also includes a watermark "20120713" and a large "WWW" watermark.

**JTB1**

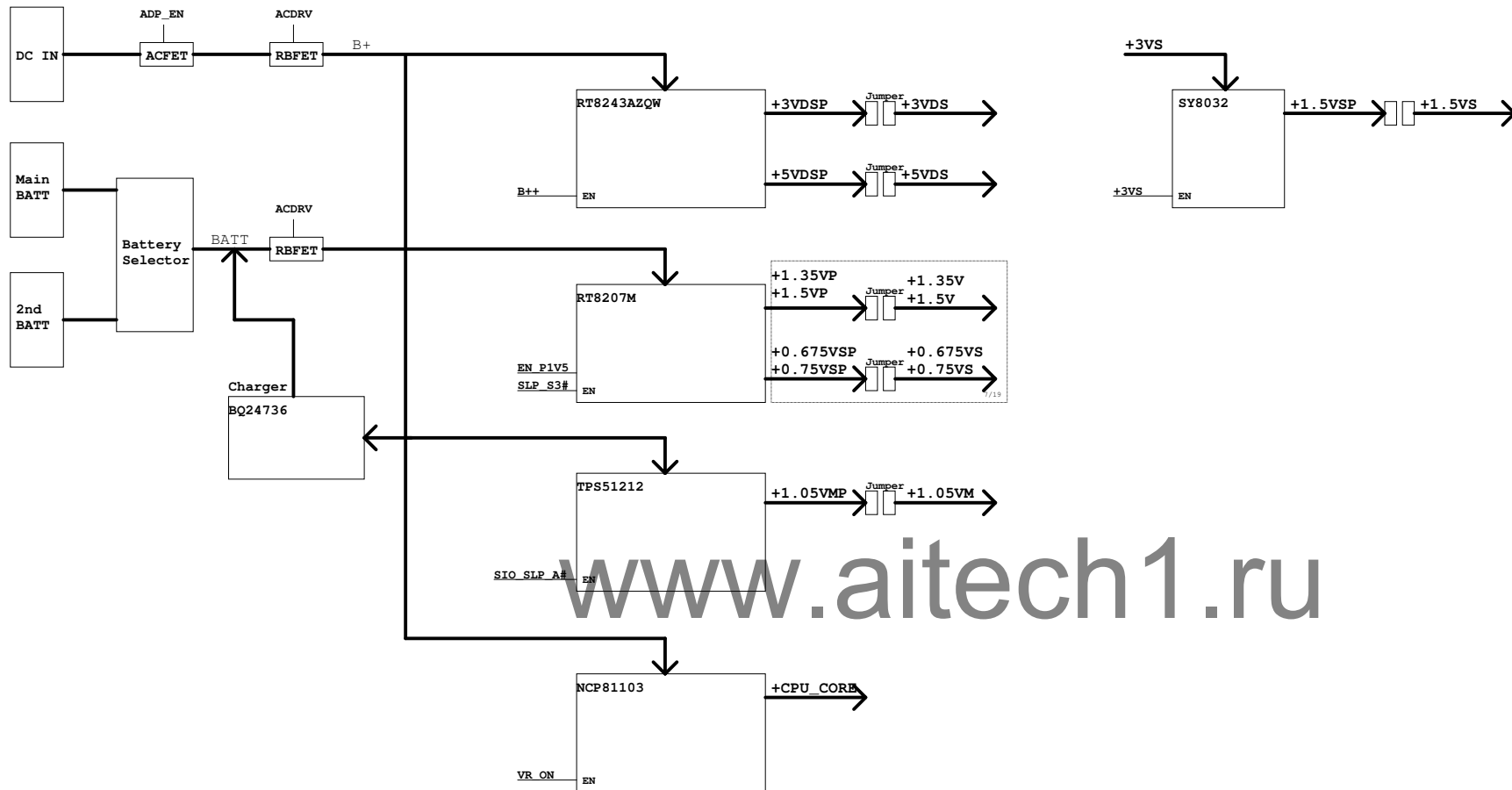
Pin	Signal	Pin	Signal	Pin	Signal
<17>	USB3T6	1	1	2	2
<17>	USB3T9	3	3	4	4
		5	5	6	6
		7	7	8	8
<17>	USB3R6	9	9	10	10
<17>	USB3RP6	11	11	12	12
		13	13	14	14
<17>	USBP5	15	15	16	16
<17>	USBP5+	17	17	18	18
		19	19	20	20
<36>	MB_DPA_AUX#	21	21	22	22
<36>	MB_DPA_AUX	23	23	24	24
		25	25	26	26
<36>	MB_DPA_TXP3	27	27	28	28
<36>	MB_DPA_TXN3	29	29	30	30
		31	31	32	32
<36>	MB_DPA_TXP2	33	33	34	34
<36>	MB_DPA_TXN2	35	35	36	36
		37	37	38	38
<36>	MB_DPA_TXP1	39	39	40	40
<36>	MB_DPA_TXN1	41	41	42	42
		43	43	44	44
<36>	MB_DPA_TXP0	45	45	46	46
<36>	MB_DPA_TXN0	47	47	48	48
		49	49	50	50
<36>	MB_DP_HPD	51	51	52	52
		53	53	54	54
<17>	USBP6	55	55	56	56
<17>	USBP6+	57	57	58	58
		59	59	60	60
<15>	CLK_PCIE_EXP#	61	61	62	62
<15>	CLK_PCIE_EXP	63	63	64	64
<15>	CLKREQ_EXP#	65	65	66	66
		67	67	68	68
<17>	PCIE_PRX_EXPTX_N5	69	69	70	70
<17>	PCIE_PRX_EXPTX_P5	71	71	72	72
		73	73	74	74
<17>	PCIE_PTX_EXPRX_N5	75	75	76	76
<17>	PCIE_PTX_EXPRX_P5	77	77	78	78
		79	79	80	80
<17>	PCIE_PRX_DTX_N2	81	81	82	82
<17>	PCIE_PRX_DTX_P2	83	83	84	84
		85	85	86	86
<17>	PCIE_PTX_C_DRX_N2	87	87	88	88
<17>	PCIE_PTX_C_DRX_P2	89	89	90	90
		91	91	92	92
7.5V	PLT_RST#	93	93	94	94
		95	95	96	96
<30>	CPPWR_EN	97	97	98	98
<14,30,31,34,4,9>	SLP_S3#	99	99	100	100
<30,33,44>	EN_PIV5	101	101	102	102
		103	103	104	104
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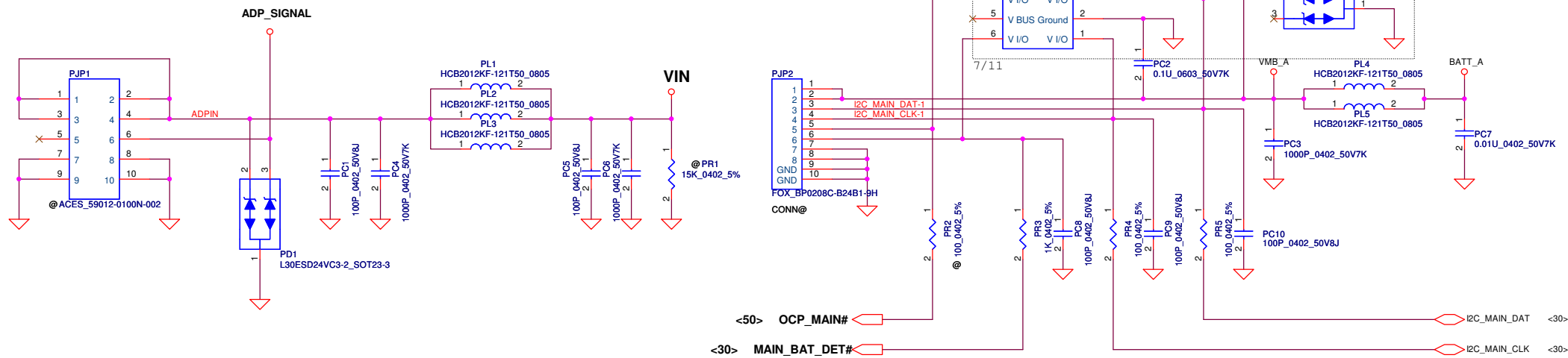
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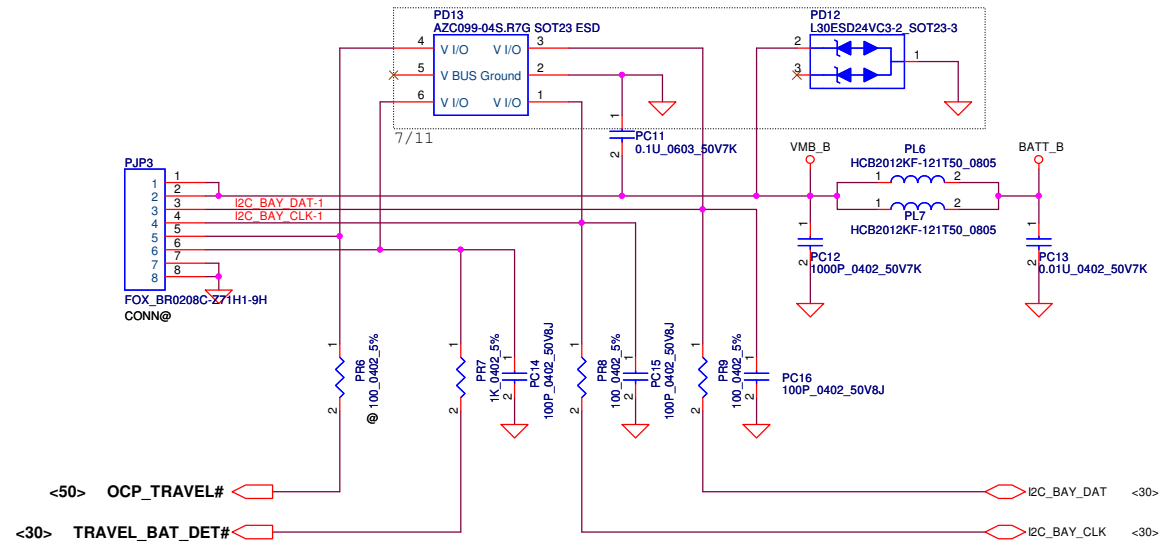


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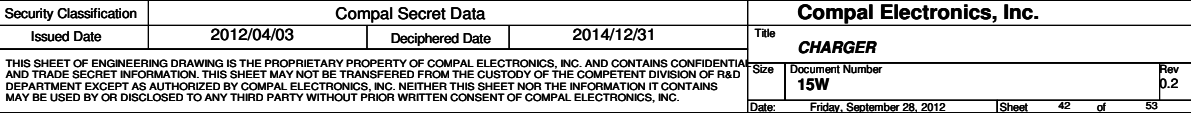


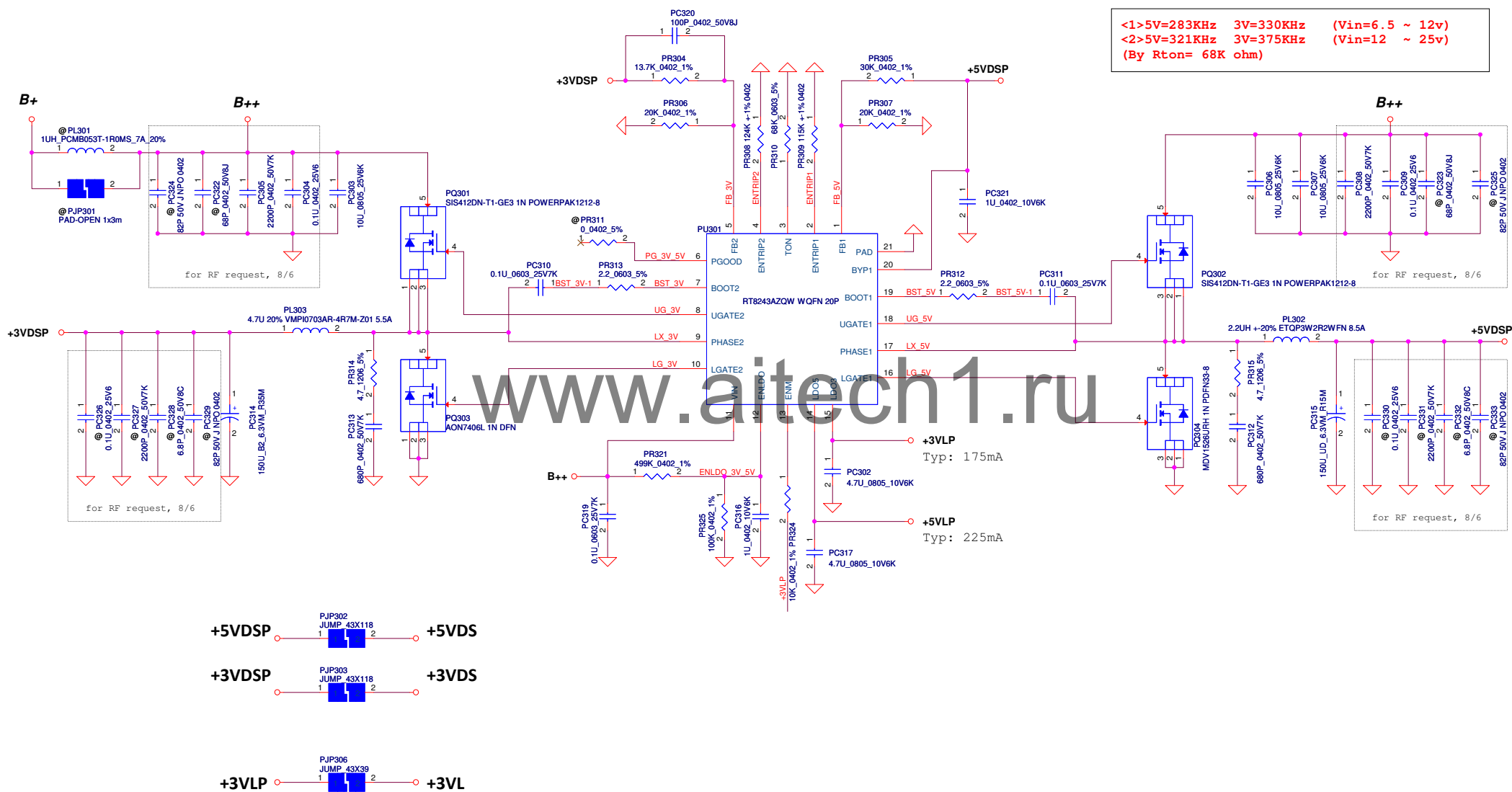


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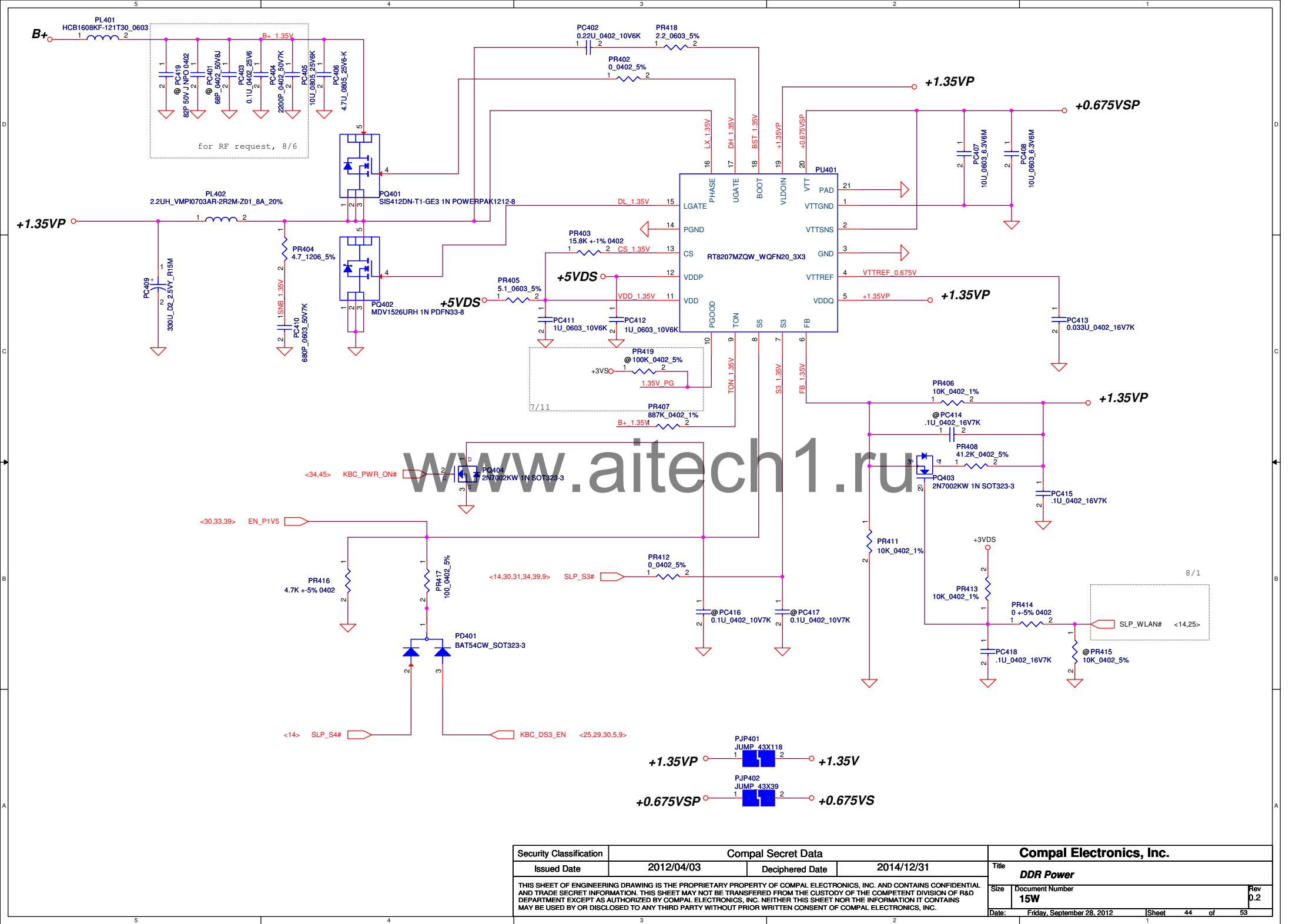
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				Date:	Friday, September 28, 2012
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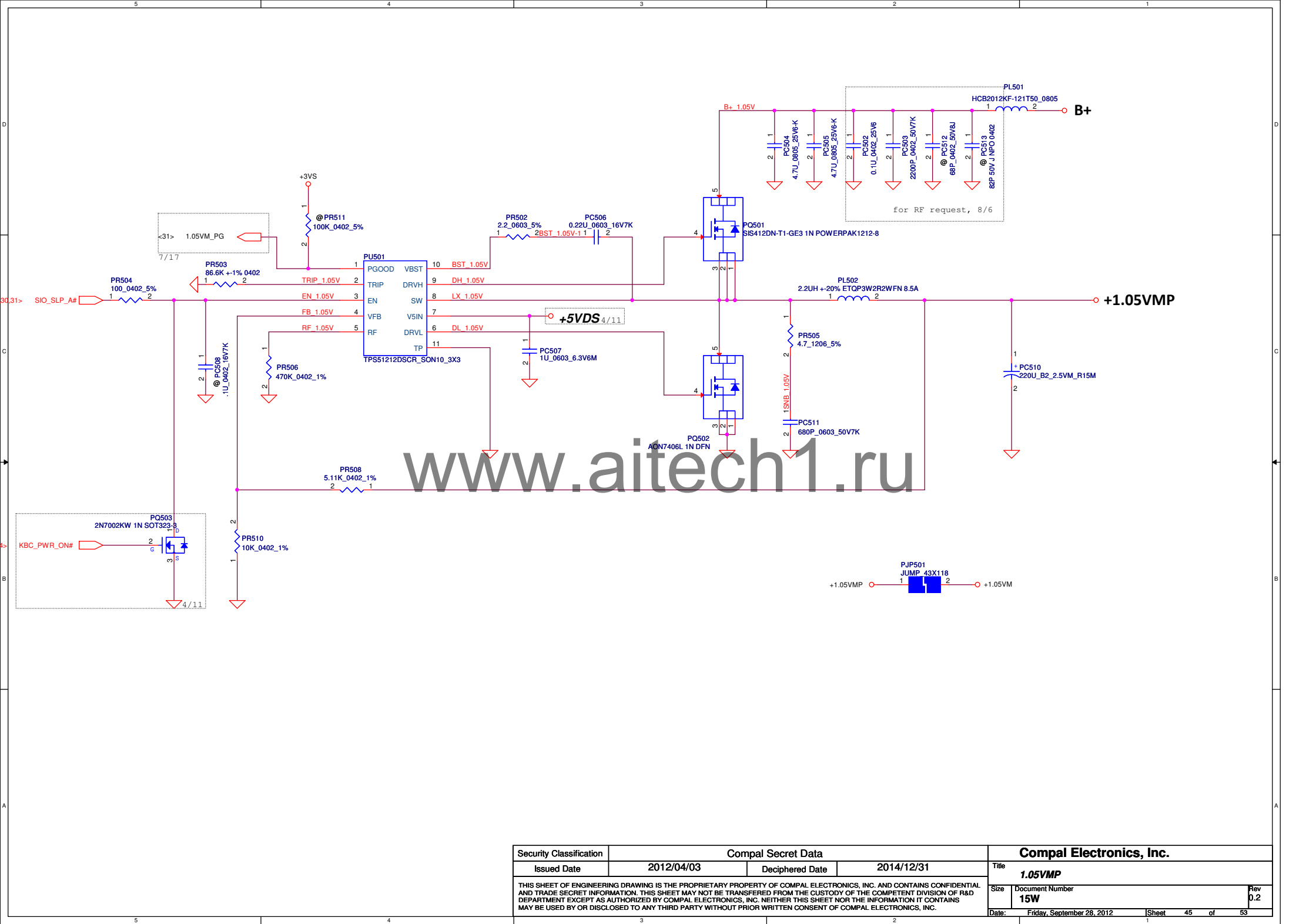


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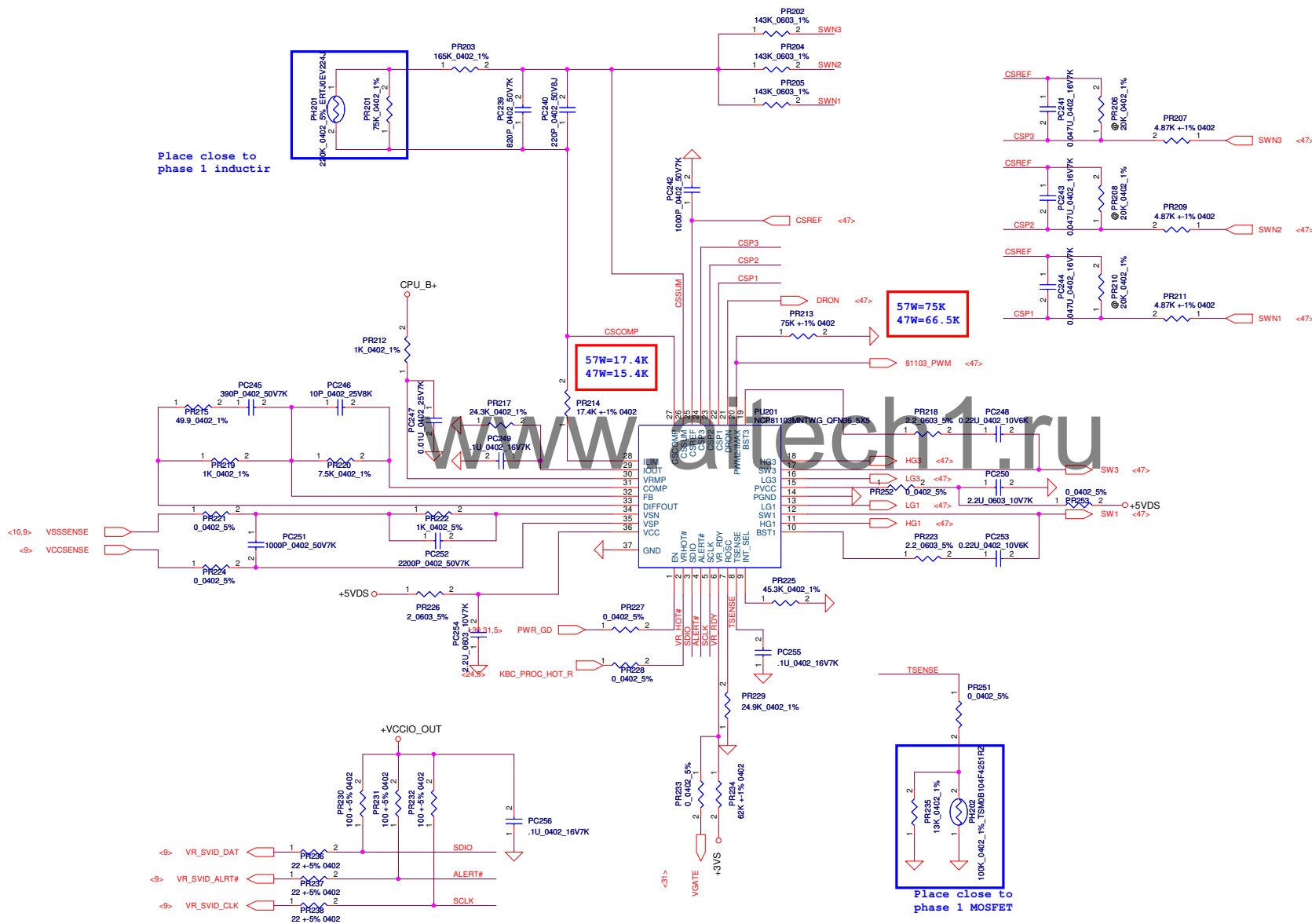




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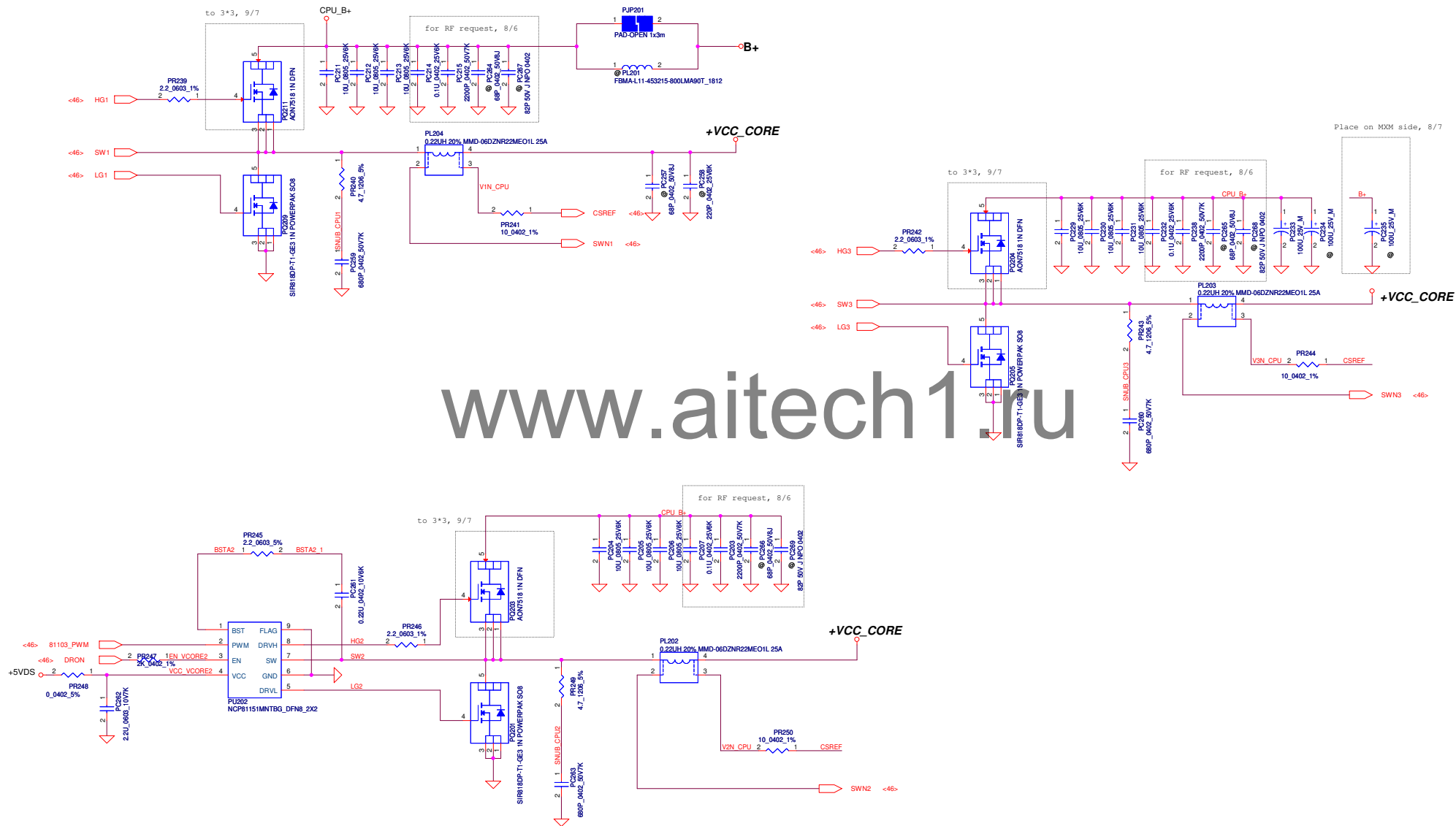


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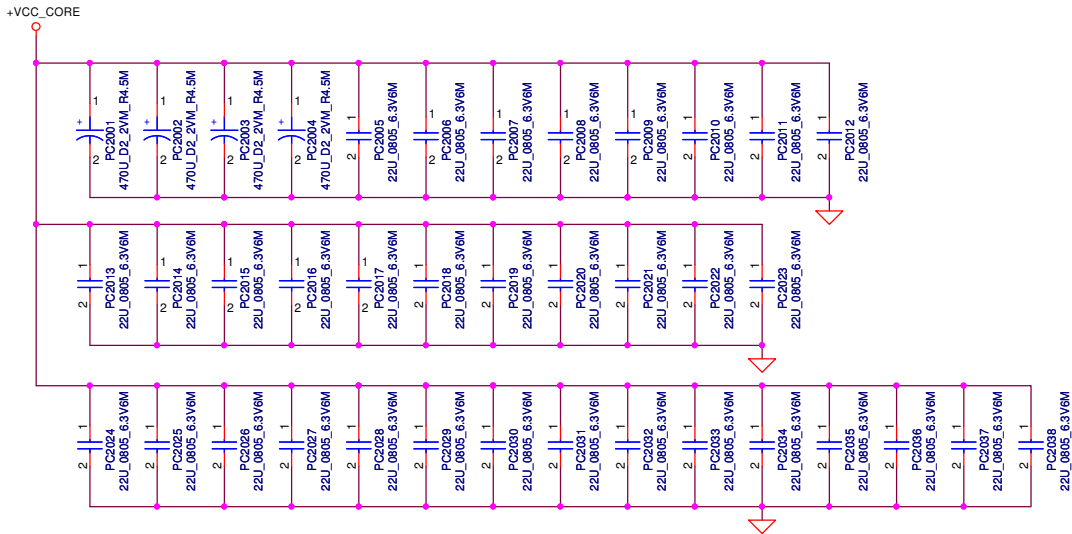
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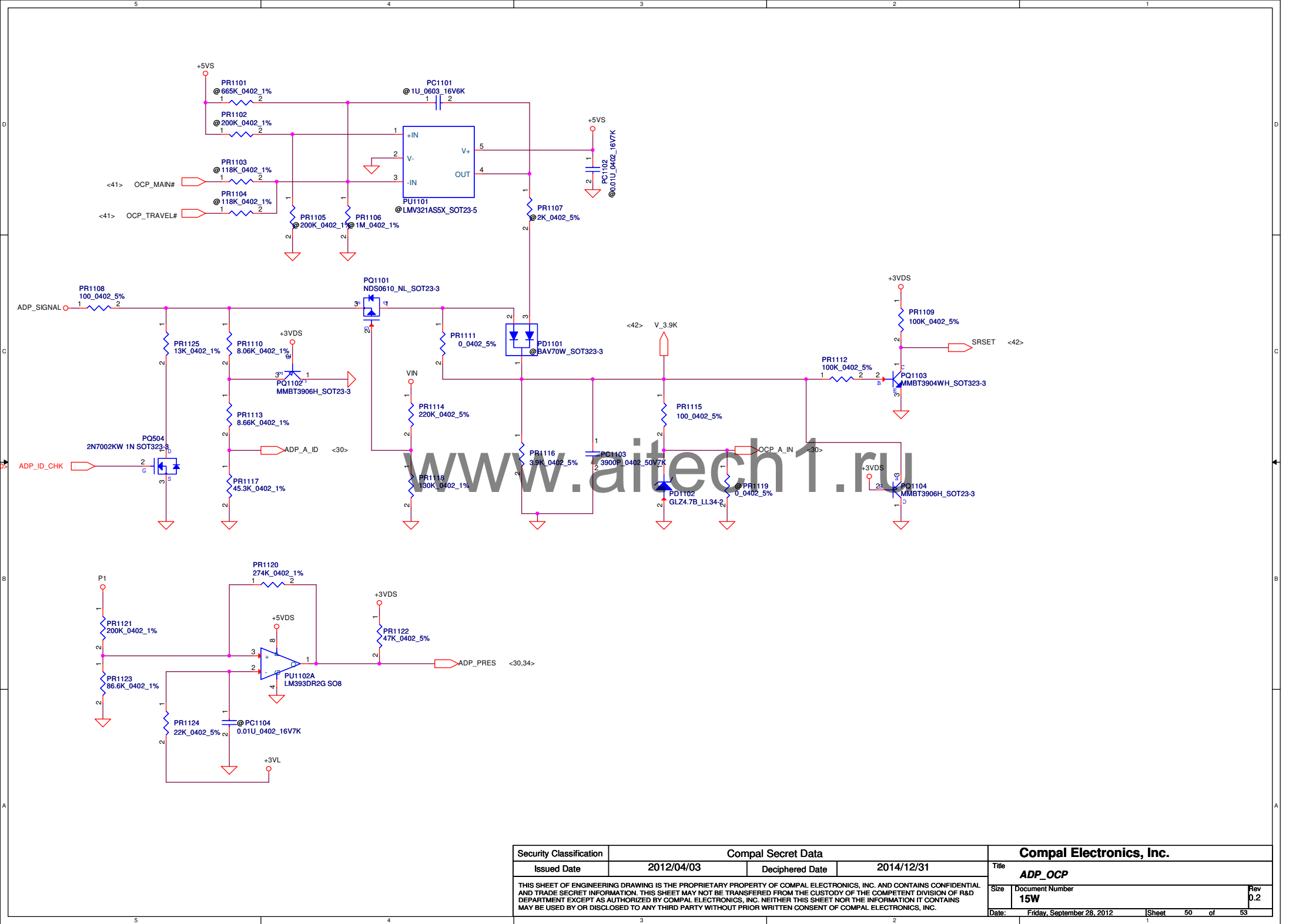
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# Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	KBC	08/18	HP	The quad-mode does not require any GPIO from KBC	Delete R1348 & R1349 and Add R541 and R542	0.2
2	31	PWR_OK	08/18	HP	Makes the power good circuit working.	Non-install R284	0.2
3	26	MXM	08/28	Compal	MXM Card can't be recognized in OS.	Change U37 to MC74VHC1G08DFT2G (Non-OD type)	0.2
4	36	Switch/MUX	09/07	HP	Move D-Sub connector on M/B	Add VGA filter circuit and connector	0.2
5	30	KBC	09/08	HP	SUSCLK is off during DS3 condition	Add Y4, C423, C424 ; Delete R258, R264	0.2
6	30	KBC	09/08	HP	Simplify the KBC solution for MEC1322	Delete R262, R266, R219, R216, R241, R242, R271, R253	0.2
7	25	NGFF	09/08	HP		Add PU resistor for WWAN_FULL_PWR/WWAN_RSVD2	0.2
8	39	NFC	09/10	HP	KBC detection of NFC module	Add 200K (R1377) PD resistor to NFC_VARI_RX	0.2
9	39	NFC	09/10	HP	Power rail option for NFC module	Add +3VM_LAN (R1376) for NFC module	0.2
10	9	CPU	09/11	HP		Remove RC102 and RC103	0.2
11	20	PCH	09/11	HP	Connect PCH's pin AD12 to +3V_PCH directly	Remove RH226	0.2
12	5	CPU	09/11	HP	Connect CPU_AT26 pin to CPU_PLTRST# directly	Remove RC66	0.2
13	5	CPU	09/11	HP	Connect CPU_AL34 pin to H_CPU_PWRGD directly	Remove RC30	0.2
14	9	CPU	09/11	HP	Connect SLP_S3# to QC5.5 directly.	Remove RC93	0.2
15	33	DOCKING	09/11	HP	Connect EN_P1V5 to JDOCK1.140 directly.	Remove R351	0.2
16	33	DOCKING	09/11	HP	Connect ON/OFFBTN_KBC# to Docking directly.	Remove R336	0.2
17	15	PCH	09/11	HP	Simplify PCH solution for PCIE CLK Group	Remove RH107, RH103, RH114, RH116, RH122 RH124, RH126, RH127, RH129, RH130	0.2
18	14	PCH	09/11	HP	Reassignment GPIO for "BT_OFF"	Change it from GPIO72 to GPIO61	0.2
19	30	KBC	09/11	HP	Reserve for SUSACK# signal	Uninstall R436 and add R1378	0.2
20	18	PCH	09/11	HP	Reassigned BRD_ID4 to GPIO40 for CP support and update table for DB1-R	Connect RH180.1 to +3VS & RPH1.8 to GND	0.2
21	30	KBC	09/12	HP	Simplify the KBC solution for MEC1322	Delete R249, R251, R256, R277	0.2
22	36	Switch/MUX	09/12	HP	eDP trace length over Intel's specification	Change solution to PS8321	0.2

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*Version Change List (P. I. R. List) for HW Circuit*

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